

Intel® 810E Chipset Platform

Design Guide

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Revision History

Revision	Description	Date
-001	Initial Release	9/99



1

Introduction

Introduction 1

This design guide provides motherboard design guidelines for Intel® 810E chipset systems. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. In addition to design guidelines, this document discusses Intel® 810E chipset system design issues (e.g., thermal requirements).

The debug recommendations should be consulted when debugging an Intel® 810E chipset system; however, the debug recommendations should be understood before completing board design to ensure that the debug port, in addition to other debug features, will be implemented correctly.

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- Chapter 1, “Introduction”—This chapter introduces the designer to the organization and purpose of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel® 810E chipset.
- Chapter 2, “PGA370 Processor Design Guidelines”—This chapter provides design guidelines for the PGA370 processor including processor-specific layout guidelines.
- Chapter 3, “SC242 Processor Design Guidelines”—This chapter provides design guidelines for the SC242 processor including processor-specific layout guidelines.
- Chapter 4, “Layout and Routing Guidelines”—This chapter provides a detailed set of motherboard layout and routing guidelines, except for processor-specific layout guidelines. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC’97, USB, interrupts, SMBUS, PCD, LPC/FWH, and RTC). For the PGA370 processor specific layout guidelines, refer to Chapter 2, “PGA370 Processor Design Guidelines”. For the SC242 processor spcific layout guidelines, refer to Chapter 3, “SC242 Processor Design Guidelines”.
- Chapter 5, “Advanced System Bus Design”—The goal of this chapter is to provide the system designer with the information needed for the implementation of 133 MHz and 100 MHz (single and dual processor) AGTL+ bus PCB layout.
- **Chapter 6, “Clocking”—** This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- Chapter 7, “System Design Considerations”— This chapter includes guidelines regarding power deliver, decoupling, thermal, and power sequencing.
- Chapter 8, “Design Checklist”— This chapter provides a design review checklist. ATA/66 detection, calculation of pullup/pulldown resistors, minimizing RTC ESD, and power management signals are also discussed.
- Chapter 9, “Flexible Motherboard Guidelines”— This chapter includes guidelines regarding power deliver, decoupling, thermal, and power sequencing.
- Chapter 10, “Third-Party Vendor Information”— This chapter includes information regarding various third-party vendors who provide products to support the Intel® 810E chipset.

- Appendix A, “PCI Devices/Functions/Registers/Interrupts”— This appendix lists the PCI devices and functions supported by the Intel® 810E chipset. Also included are a list of component PCI Vendor ID, Device ID, Revision ID, Class code, Sub-class code, and Programming Interface code values. In addition, component APIC interrupt and ISA/PCI IRQs are listed.

1.1.1 Terminology and Definitions

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Additionally, the processor Single Edge Connector (S.E.C.) cartridge contains 56 Ω pull-up resistors to provide termination at each bus load.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.

Term	Definition
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Cross-talk - coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Cross-talk - coupling which creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation.
Edge Finger	The cartridge electrical contact that interfaces to the SC242 connector.

Term	Definition
Flight Time	Flight Time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: • The time difference between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.), and the output pin of the driving agent crossing V_{REF} if the driver was driving the Test Load used to specify the driver's AC timings. See Section for details regarding flight time simulation and validation. The V_{REF} Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the V_{REF} Guardband. • **Maximum and Minimum Flight Time** - Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, cross-talk, V_{TT} noise, V_{REF} noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of *Simultaneous Switching Output (SSO)* and packaging effects. • The **Maximum Flight Time** is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate V_{REF} Guardband boundary. • The **Minimum Flight Time** is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate V_{REF} Guardband boundary. For more information on flight time and the V_{REF} Guardband, see the *Pentium® II Processor Developer's Manual.*
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state (S0) and the processor Stop Grant state (S1).
GTL+	GTL+ is the bus technology used by the Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the *Pentium® II Processor Developer's Manual* for more details of GTL+.
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.

Term	Definition
Overdrive Region	Is the voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Pentium® II Processor Developer's Manual* for more details.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each process's *Electrical, Mechanical, and Thermal Specification* for overshoot specification.
Pad	A feature of a semiconductor die contained within an internal logic package on the S.E.C cartridge substrate used to connect the die to the package bond wires. A pad is only observable in simulation.
Pin	A feature of a logic package contained within the S.E.C. cartridge used to connect the package to an internal substrate trace.
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, +5VSB. In addition to these power rails, several other power rails can be created with voltage regulators.
Ringback	Ringback is the voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective *Processor's Electrical, Mechanical, and Thermal Specification* for ringback specification.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective *Processor's Electrical, Mechanical, and Thermal Specification* for settling limit specification.
Setup Window	Is the time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is 5VSB (5V Standby). There can be other standby rails that are created with voltage regulators.
Stub	The branch from the trunk terminating at the pad of an agent.
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: processor Stop Grant (S1), Suspend-to-RAM (S3) and Soft-off (S5).

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below V_{SS} at the processor core pad. See the respective *Processor's Electrical, Mechanical, and Thermal Specification* for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (DV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

1.1.2 References

- *Intel® 82810 Chipset: Intel® 82810/82810-DC100 Graphics and Memory Controller (GMCH)* Datasheet (Order Number: 290656)
- *Intel® 82801AA (ICH) and 82810AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® 82801 FirmWare Hub (FWH) Datasheet* (Order Number: 290658)
- *Intel® Celeron Processor Datasheet* (Order Number: 243658)
- *Intel® Celeron Processor Specification Update* (Order Number: 243748)
- *Intel® 810E Chipset Clock Synthesizer/Driver Specification*
- *PPGA 370 Power Delivery Guidelines*
- *Intel® Pentium® II Processor AGTL+ Guidelines* (Order Number: 243330)
- *Intel® Pentium® II Processor Power Distribution Guidelines (*Order Number: 243332)
- *Intel® Pentium® II Processor Developer's Manual* (Order Number: 243341)
- *Intel® Pentium® II Processor at 350MHz, 400MHz and 450MHz Datasheet* (Order Number: 243657)
- *Intel® Pentium® II Processor Specification Update* (Order Number: 243337)
- *Intel® Pentium® III Processor Datasheet* (Order Number: 244452)
- *Intel® Pentium® III Processor Specification Update* (Order Number: 244453)
- *AP-907: Intel®Pentium® III Power Distribution Guidelines* (Order Number: 245085)
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0

1.2 System Overview

The Intel® 810E chipset enhances the performance of the first generation Integrated Graphics chipset designed for the Intel® Celeron™ and Intel® Pentium III®processors. The graphics accelerator architecture consists of dedicated multi-media engines executing in parallel to deliver high performance 3D, 2D, and motion compensation video capabilities. An integrated centralized memory arbiter allocates memory bandwidth to multiple system agents to optimize system memory utilization. A new chipset component interconnect, the hub interface, is designed into the Intel® 810E chipset to provide an efficient communication channel between the memory controller hub and the I/O hub controller.

The Intel® 810E chipset architecture also enables a new security and manageability infrastructure through the Firmware Hub component.

An ACPI compliant Intel® 810E chipset platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. Through the use of an appropriate LAN device, the Intel® 810E chipset also supports *wake-on-LAN** for remote administration and troubleshooting.

The Intel® 810E chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The

elimination of ISA provides true *plug-and-play* for the Intel® 810E chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software configurable* AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

The Intel® 810E Chipset contains three core components:

- Graphics and Memory Controller Hub (GMCH)
  - 82810E
- I/O Controller Hub (ICH)
  - 82801AA
- Firmware Hub (FWH)
  - 82802

The GMCH integrates a 66/100/133MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator, 100 MHz SDRAM controller and a high-speed hub interface for communication with the I/O Controller Hub (ICH). The integrates an Ultra ATA/66 controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the GMCH.

1.2.1 Graphics and Memory Controller Hub (GMCH)

The GMCH provides the interconnect between the SDRAM and the rest of the system logic:

- 421 Mini BGA
- Integrated Graphics controller
- 230 MHz RAMDAC
- Support for Intel® Celeron™ and Intel® Pentium III®processors with a 66, 100 or 133 MHz system bus.
- 100 MHz SDRAM interface supporting 64 MB/256 MB/512 MB with 16Mb/64Mb/128Mb SDRAM technology
- Optional 100/133MHz 4 MB Display Cache
- Downstream hub interface for access to the ICH
- TV-Out/Flat Panel Display support

1.2.2 I/O Controller Hub (82801AA ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system:

- 241 Mini BGA
- Upstream hub interface for access to the GMCH
- PCI 2.2 interface with 6 PCI Req/Grant Pairs
- Bus Master IDE controller; supports Ultra ATA/66.
- USB controller
- SMBus controller
- FWH interface
- LPC interface
- AC’97 2.1 interface
- Integrated System Management Controller
- Alert-on-LAN
- Interrupt controller

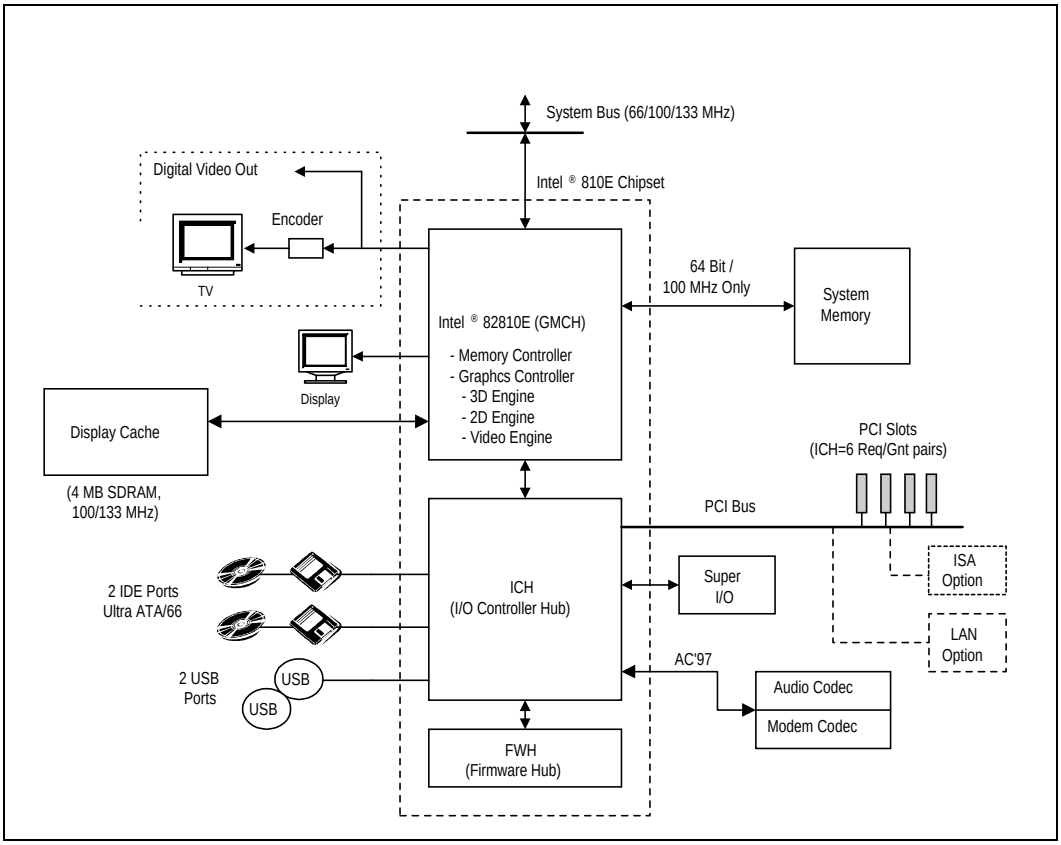
1.2.3 Firmware Hub (82802 FWH)

The 82802 FWH component is a key element to enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPI’s

1.2.4 System Configurations

Figure 1-1. Intel® 810E Chipset



1.3 Platform Initiatives

1.3.1 Hub Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and Ultra ATA/66, coupled with the existing USB, I/O requirements could impact PCI bus performance. The Intel® 810E Chipset's *hub interface architecture* ensures that the I/O subsystem (both PCI and the integrated I/O features (IDE, AC'97, USB, etc.)), receives adequate bandwidth. By placing the I/O bridge on the hub interface (instead of PCI), the hub architecture ensures that both the I/O functions integrated into the ICH and the PCI peripherals obtain the bandwidth necessary for peak performance.

1.3.2 Manageability

The Intel® 810E chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH can be programmed to generate an SMI# or TCO event due to an active INTRUDER# signal.

Alert-On-LAN*

The ICH supports Alert-On-LAN*. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH sends a hardcoded message over the SMBus. A LAN controller supporting the Alert-On-LAN* protocol can decode this SMBus message and send a message over the network to alert the network manager.

1.3.3 AC'97

The *Audio Codec '97* (AC'97) Specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC'97 Digital Link*.

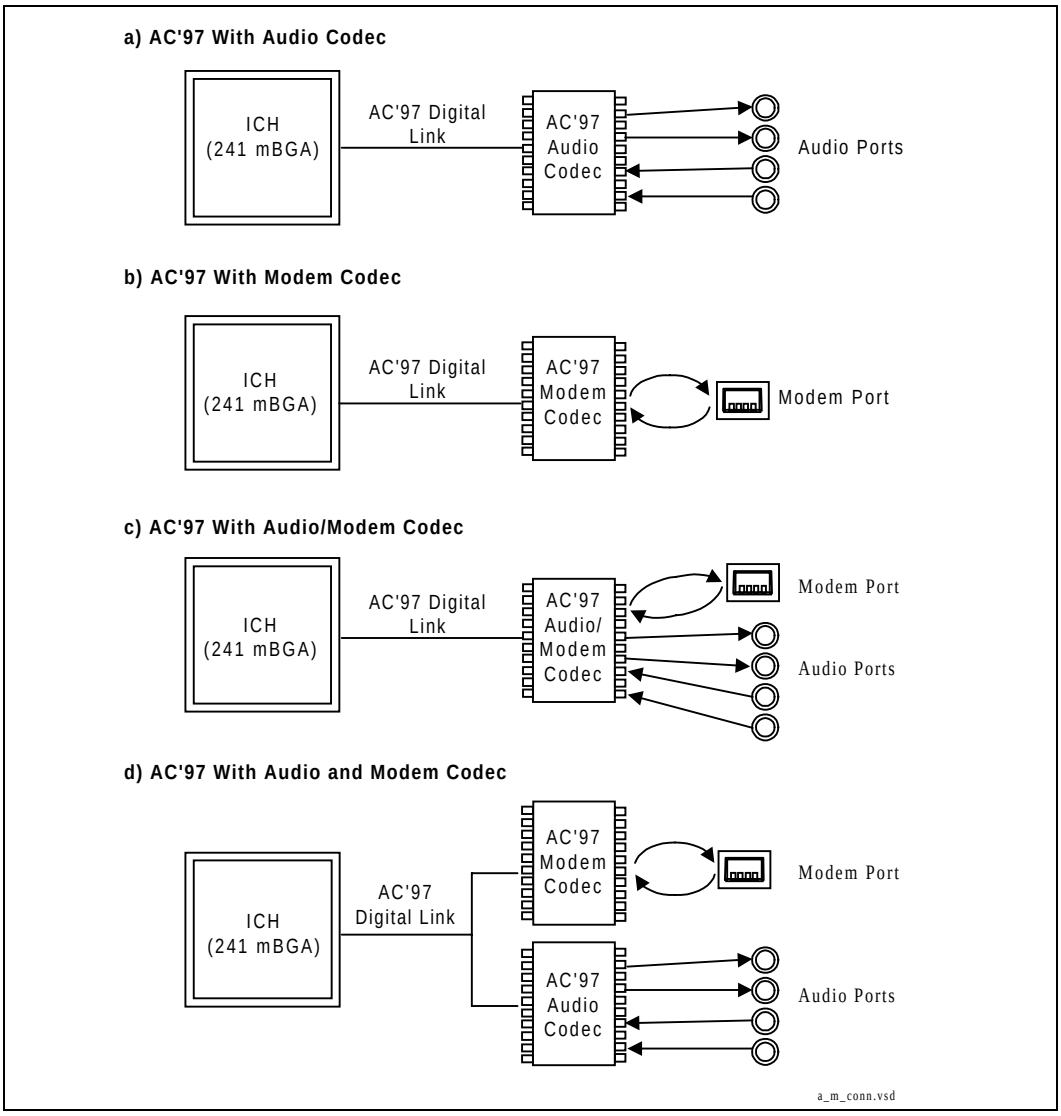
The ability to add cost-effective audio and modem solutions as the platform migrates away from ISA is important. The AC'97 audio and modem components are software configurable, reducing configuration errors. The Intel® 810E chipset's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC'97 digital link. Using the Intel® 810E chipset's integrated AC'97 digital link reduces cost and eases migration from ISA.

The ICH is an AC'97 compliant controller that supports up to two codecs with independent PCI functions for audio and modem. The ICH communicates with the codec(s) via a digital serial link called the AC-link. All digital audio/modem streams and command/status information is communicated over the AC-link. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 810E chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. The Intel® 810E chipset's integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec (Figure 1-2 a) or a modem with a modem codec (Figure 1-2 b). For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into an AMC (Figure 1-2 c), or separate audio and modem codecs can be connected to the ICH (Figure 1-2 d).

The modem implementation for different countries should be considered as telephone systems vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC'97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

Figure 1-2. AC'97 with Audio and Modem Codec Connections



1.3.4 Low Pin Count (LPC) Interface

In the Intel® 810E chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of devices offered and features supported.

In addition, depending on system requirements, a device bay controller and USB hub could be integrated into the LPC Super I/O component. For systems requiring ISA support, an ISA-IRQ to serial-IRQ converter is required. Potentially, this converter could be integrated into the Super I/O.

1.3.5 Security – the Intel® Random Number Generator

The Intel® 810E chipset features the first of Intel's platform security features, the Intel Random Number Generator (RNG). The Intel RNG is a component of the 82802 Firmware Hub (FWH), and it supplies applications and security middleware products with true non-deterministic random numbers (through the Intel® Security Driver).

Better random numbers lead to better security. Most cryptographic functions, especially functions that provide authentication or encryption services, require random numbers for purposes such as key generation. One attack on those cryptographic functions is to predict the random numbers being used to generate those keys; current methods that use system and user input to seed a pseudo random number generator have shown to be susceptible to those attacks. The Intel® RNG uses thermal noise across a resistor to generate true non-deterministic, unpredictable random numbers.

2

PGA370 Processor Design Guidelines

PGA370 Processor Design Guidelines 2

This chapter provides PGA370 processor design guidelines including the PGA370 socket, Layout Guidelines, BSEL implementation, CLKREF, Undershoot/Overshoot requirements, Reset, Decoupling guidelines, Thermal/EMI differences, and Debug Port changes. The layout guidelines are processor-specific and should be used in conjunction with the Chapter 4, "Layout and Routing Guidelines". For this chapter, the following terminology applies:

- *Legacy PGA370* refers to today's Intel® 810 chipset platforms utilizing the PGA370 socket for the microprocessor. In general, these designs support 66/100 MHz host bus operation, *VRM 8.2 DC-DC Converter Guidelines*, and Intel® Celeron™ processors.
- *Flexible PGA370* refers to new generation Intel® 810/810E chipset platforms utilizing the PGA370 socket and designed for microprocessor flexibility. In general, these designs support 66/100/133 MHz host bus operation, *VRM 8.4 DC-DC Converter Guidelines* and Intel® Celeron™, and Intel® Pentium® III Processor PGA single processor based designs.

2.1 Electrical Differences for Flexible PGA370 Designs

There are several electrical changes between the legacy and flexible PGA370 design. They include:

- Changes to the PGA370 socket pin definitions. Intel® Pentium® III processors utilize a superset of the Intel® Celeron™ processor pin definition.
- Addition of VTT (AGTL+ termination voltage) delivery to the PGA370 socket.
- BSEL[1:0] implementation differences. BSEL1 has been added to select either a 100 MHz or 133 MHz host bus frequency setting from the CK810E clock synthesizer.
- Additional PLL reference voltage, 1.25V, on new CLKREF pin.
- More stringent undershoot/overshoot requirements for CMOS and AGTL+ signals.
- Addition of on-die Rtt (AGTL+ termination resistors) for the Intel® Pentium® III processor. Requirement remains for on-motherboard Rtt implementation if supporting the Intel® Celeron™ (PPGA). If only supporting Intel® Pentium® III processors, the reset signals (RESET#) still requires termination to V_{TT} on the motherboard.

2.2 PGA370 Socket Definition Details

The following tables compare legacy pin names and functions to new flexible pin names and functions. Designers need to pay close attention to the notes section for this table for compatibility concerns regarding these pin changes.

Table 2-1. Platform Pin Definition Comparison for Single Processor Designs

Pin #	Legacy PGA370 pin name	Flexible PGA370 pin name	Function	Type	Notes
A29	Reserved	DEP7#	Data bus ECC data	AGTL+, I/O	2
A31	Reserved	DEP3#	Data bus ECC data	AGTL+, I/O	2
A33	Reserved	DEP2#	Data bus ECC data	AGTL+, I/O	2
AC1	Reserved	A33#	Additional AGTL+ address	AGTL+, I/O	2
AC37	Reserved	RSP#	Response parity	AGTL+, I	2
AF4	Reserved	A35#	Additional AGTL+ address	AGTL+, I/O	2
AH20	Reserved	VTT	AGTL+ termination voltage	Power	
AH4	Reserved	RESET#	Processor reset (Intel® Pentium® III)	AGTL+, I	3
AJ31	GND	BSEL1	System bus frequency select	CMOS, I/O	1
AK16	Reserved	VTT	AGTL+ termination voltage	Power	
AK24	Reserved	AERR#	Address parity error	AGTL+, I/O	2
AL11	Reserved	AP0#	Address parity	AGTL+, I/O	2
AL13	Reserved	VTT	AGTL+ termination voltage	Power	
AL21	Reserved	VTT	AGTL+ termination voltage	Power	
AM2	GND	Reserved	Reserved	Reserved	1
AN11	Reserved	VTT	AGTL+ termination voltage	Power	
AN13	Reserved	AP1#	Address parity	AGTL+, I/O	2
AN15	Reserved	VTT	AGTL+ termination voltage	Power	
AN23	Reserved	RP#	Request parity	AGTL+, I/O	
B36	Reserved	BINIT#	Bus initialization	AGTL+, I/O	2
C29	Reserved	DEP5#	Data bus ECC data	AGTL+, I/O	2
C31	Reserved	DEP1#	Data bus ECC data	AGTL+, I/O	2
C33	Reserved	DEP0#	Data bus ECC data	AGTL+, I/O	2
E29	Reserved	DEP6#	Data bus ECC data	AGTL+, I/O	2
E31	Reserved	DEP4#	Data bus ECC data	AGTL+, I/O	2
G35	Reserved	VTT	AGTL+ termination voltage	Power	
V4	Reserved	BERR#	Bus error	AGTL+, I/O	2
W3	Reserved	A34#	Additional AGTL+ address	AGTL+, I/O	2
X4	RESET#	RESET2#	Processor reset (Value processors)	AGTL+, I	3
X6	Reserved	A32#	Additional AGTL+ address	AGTL+, I/O	2
Y33	GND	CLKREF	1.25V PLL reference	Power	1

NOTES:
1. These signals were previously defined as ground (Vss) connections in legacy designs utilizing the PGA370 socket to provide termination for unused inputs. For new *Flexible PGA370* designs, use the new signal definitions. These new signal definitions are backwards compatible with the Intel® Celeron™ processor (PPGA).
2. While these signals are not used with Intel® 810E chipset designs, they are available for chipsets that do support these functions. Only the Intel® Pentium® III processor offers these capabilities in the PGA370 platform.
3. The AGTL+ reset signal, RESET#, is delivered to pin X4 on *Legacy PGA370* designs. On *Flexible PGA370* designs it is delivered to X4 and AH4 pins. See Figure 2-1 for more details.

2.2.1 Layout Guidelines for Intel® Pentium® III Processors

The following layout guide supports designs using Intel® Celeron™ processors and Intel® Pentium® III processor with the Intel® 810E chipset. The solution covers system bus speeds of 66 MHz for the Intel® Celeron™ processor and 100/133 MHz for the Intel® Pentium® III processors. The solution proposed in this segment requires the motherboard design to terminate the system bus AGTL+ signals with a 56 Ω ±5% Rtt. The Intel® Pentium® III processor must also be configured to 110 Ω internal Rtt.

Initial Timing Analysis

Table 2-2 lists the AGTL+ component timings of the processors and 82810E GMCH defined at the pins. **These timings are for reference only; obtain each processor's specifications from its respective processor Electrical, Mechanical, and Thermal Specification and appropriate Intel® 810E Chipset component specification.**

Table 2-2. Intel® Pentium® III Processor and Intel® 810E GMCH AGTL+ Parameters for Example Calculations

IC Parameters	Intel® Pentium® III Processor Core at 133 MHz System Bus	Intel® 82810E GMCH at 133MHz System Bus	Notes
Clock to Output maximum (T_{CO_MAX})	2.70	3.70	2
Clock to Output minimum (T_{CO_MIN})	0.20	0.5	2
Setup time (T_{SU_MIN})	1.20	2.72	2,3
Hold time (T_{HOLD})	1.0	0.10	

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 2.72 ns assumes the Intel® 810E GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 2-3 gives an example AGTL+ initial maximum flight time and Table 2-4 is an example minimum flight time calculation for a 133 MHz processor system using the Intel® Pentium® III processor/Intel® 810E chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

Table 2-3 and Table 2-4 are derived assuming:

- CLK_{SKEW} = 0.20 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets *the CK810E Clock Synthesizer/ Driver Specification* is being used.)
- CLK_{JITTER} = 0.250 ns

See the appropriate Intel® 810E chipset documentation, and *CK810E Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

Table 2-3. Example T_{FLT_MIN} Calculations FOR 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	Intel® 810E GMCH	7.50	2.70	2.72	0.20	0.25	0.40	3.73
Intel® 810E GMCH	Processor	7.50	5.35	1.20	0.20	0.25	0.40	2.60

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   - The effective board propagation constant (S_{EFF}), which is a function of:
     — Dielectric constant (ε_r) of the PCB material.
     — The type of trace connecting the components (stripline or microstrip).
     — The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

Table 2-4. Example T_{FLT_MIN} Calculations (Frequency Independent)[1]

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	Clk_{SHIFT}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	82810E GMCH	0.10	0.15	0.35	0.20	0.40
82810E GMCH	Processor	1.0	0.15	0.35	1.27	0.23

NOTES:
1. All times in nanoseconds.

2.2.1.1 Determine General Topology and Layout

In the SET (Single Ended Termination) topology for the 370-pin socket (PGA370), the termination should be placed close to the processor on the motherboard. There is no termination present at the chipset end of the network. Due to the lack of termination, SET will exhibit much more ringback than the dual terminated topology. Extra care is required in SET simulations to make sure that the ringback specs are met under the worst case signal quality conditions. Intel® 810E chipset designs require all AGTL+ signals to be terminated with a 56 Ω termination on the motherboard. To ensure processor signal integrity requirements **it is highly recommended that all system bus signal segments to be referenced to the ground plane for the entire route (Chapter 5, "Advanced System Bus Design" for details).**

Figure 2-1. Topology for 370-Pin Socket Designs with Single Ended Termination (SET)

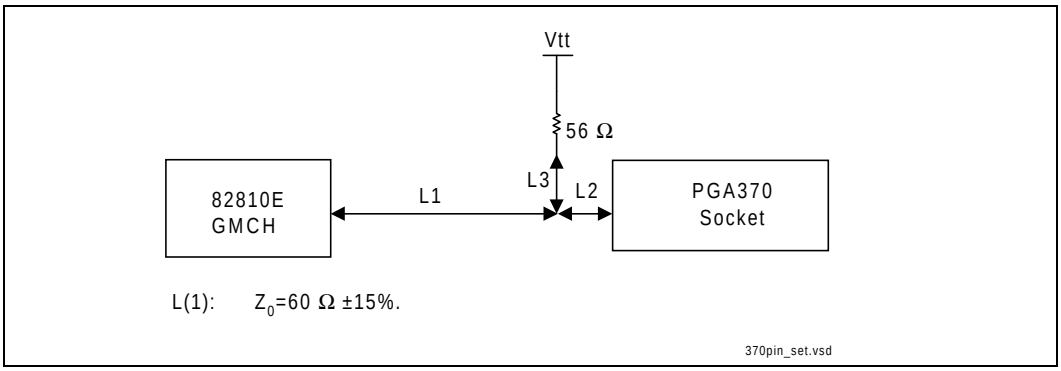


Table 2-5. Segment Descriptions and Lengths for Figure 2-1 [1]

Segment	Description	Min length (inches)	Max length (inches)
L1	82810E GMCH to Rtt Stub	1.90	4.50
L2	PGA370 Pin to Rtt stub	0.0	0.20
L3	Rtt Stub length	0.50	2.50

NOTES:
1. All AGTL+ bus signals should be referenced to the ground plane for the entire route. See Chapter 5, "Advanced System Bus Design".

- AGTL+ signals should be routed with trace lengths within the range specified for L1+L2 from the processor pin to the chipset.
- Use an intragroup AGTL+ spacing to line width to dielectric thickness ratio of at least 2:1:1 for microstrip geomety. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
- The trace width is recommended to be 5 mils and not greater than 6 mils.

Table 2-6 contains the trace width:space ratios assumed for this topology. The crosstalk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intragroup AGTL+ crosstalk involves interference between AGTL+ signals within the same group. Intergroup AGTL+ crosstalk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ crosstalk is when CMOS and AGTL+ signals interfere with each other.

Table 2-6. Trace Width:Space Guidelines

Crosstalk Type	Trace Width:Space Ratios
Intragroup AGTL+ signals (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ signals (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

2.2.1.2 Motherboard Layout Rules for AGTL+ Signals

Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

2.2.1.3 Motherboard Layout Rules for Non-AGTL+ (CMOS) Signals

Non-AGTL+ (CMOS) Signals

Route these signals on any layer or any combination of layers.

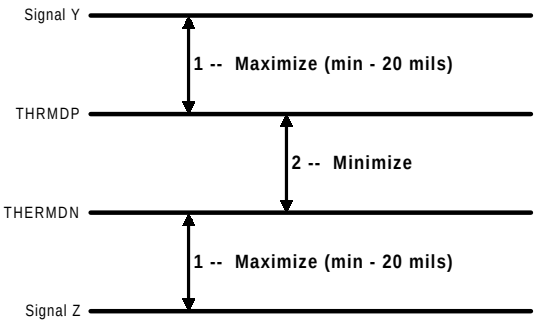
Table 2-7. Routing Guidelines for Non-AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 6”
FERR#	5 mils	10 mils	1” to 6”
FLUSH#	5 mils	10 mils	1” to 6”
IERR#	5 mils	10 mils	1” to 6”
IGNNE#	5 mils	10 mils	1” to 6”
INIT#	5 mils	10 mils	1” to 6”
LINT[0] (INTR)	5 mils	10 mils	1” to 6”
LINT[1] (NMI)	5 mils	10 mils	1” to 6”
PICD[1:0]	5 mils	10 mils	1” to 8”
PREQ#	5 mils	10 mils	1” to 6”
PWRGOOD	5 mils	10 mils	1” to 6”
SLP#	5 mils	10 mils	1” to 6”
SMI#	5 mils	10 mils	1” to 6”
STPCLK	5 mils	10 mils	1” to 6”
THERMTRIP#	5 mils	10 mils	1” to 6”

2.2.1.4 THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance (Refer to Figure 2-2).

Figure 2-2. Routing for THRMDP and THRMDN



- Rule
  - — Length Equalization route these traces parallel ±0.5”
  - — Layer route both on the same layer

2.2.1.5 Additional Considerations

- Distribute Vtt with a wide trace. A 0.050" minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include decoupling capacitors.
- The V_{TT} voltage should be 1.5V ±3% for static conditions, and 1.5V ±9% for transient condition.
- Place resistor divider pairs for V_{REF} generation at the 82810E GMCH component. V_{REF} is also delivered to the processor.

2.2.2 Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

2.2.3 BSEL[1:0] Implementation for PGA370 Designs

The Intel® Pentium® III processor utilizes the BSEL1 pin to select either a 100 MHz or 133 MHz system bus frequency setting from the CK810E clock synthesizer. While the BSEL0 signal is still connected to the PGA370 socket, the Intel® Pentium® III processor does not utilize it. Only the Intel® Celeron™ processor (PPGA) utilizes the BSEL0 signal. The Intel® Pentium® III processors are 3.3V tolerant for these signals, as are the CK810E and GMCH. However, the Intel® Celeron™ processor requires 2.5V logic levels on the BSEL signals.

A new clock synthesizer, the CK810E, has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. This maintains pin compatibility with the CK810 clock synthesizer. Figure 2-3 details the new BSEL[1:0] circuit design for *Flexible PGA370* designs. **Note that BSEL[1:0] are now pulled up using 1 KΩ resistors.** Figure 2-3 shows the 82810E GMCH and Processor straps for selecting the system bus frequency:

Figure 2-3. BSEL[1:0] Circuit Implementation for PGA370 Designs

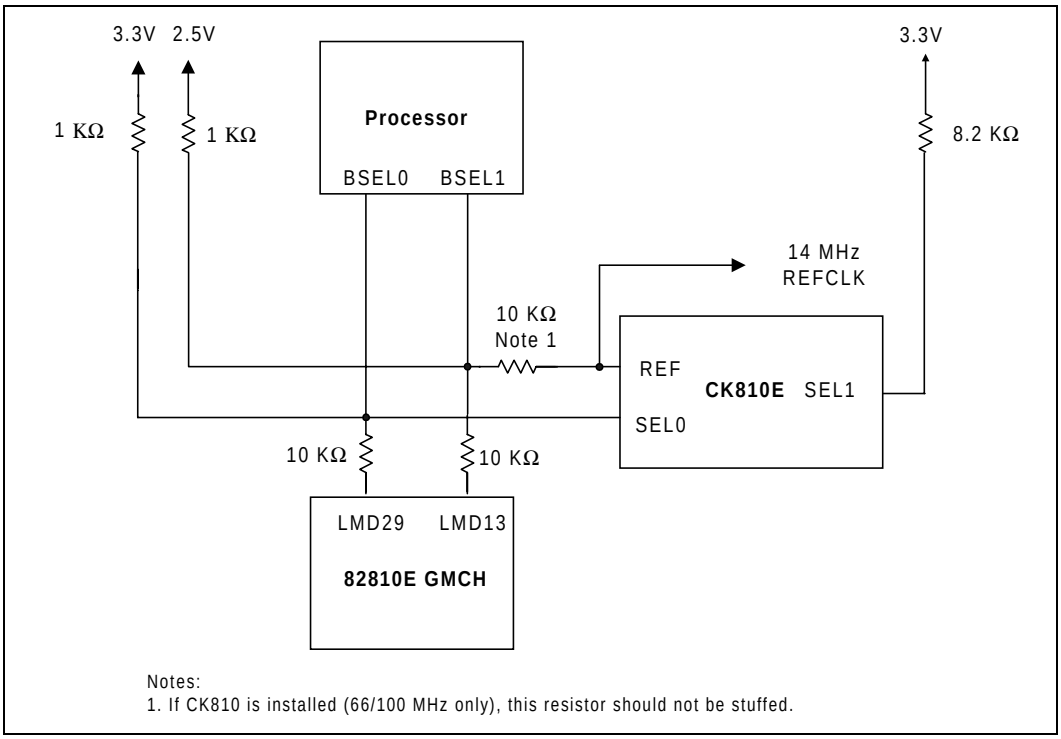


Table 2-8. CK810E Reset Strapping Matrix

REF	SEL1	SEL0	CK810E FUNCTION
X	0	0	Tristate
X	0	1	Test
0	1	0	Active CPU = 66 MHz
0	1	1	Active CPU = 100 MHz
1	1	1	Active CPU = 133 MHz
1	1	0	Reserved

2.2.4 CLKREF Circuit Implementation

The CLKREF input requires a 1.25V source. It can be generated from a voltage divider on the Vcc2.5 or Vcc3.3 sources utilizing 1% tolerance resistors. A 4.7 uF decoupling capacitor should be included on this input. See Figure 2-4 and Table 2-9 for example CLKREF circuits. **Do not use Vtt as the source for this reference!**

Figure 2-4. Examples for CLKREF Divider Circuit

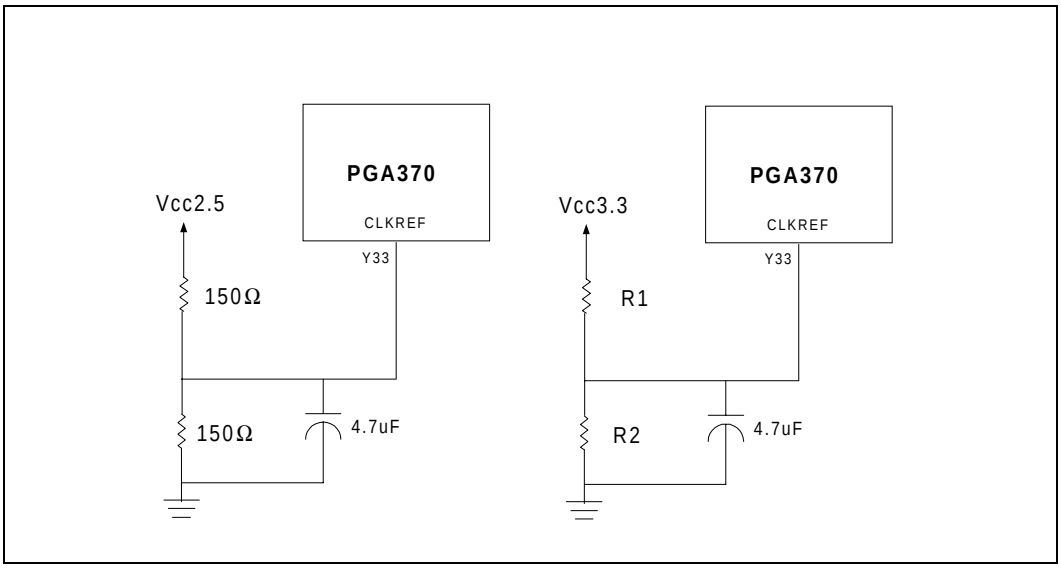


Table 2-9. Example Resistor Values for CLKREF Divider Circuit 3.3V Source)

R1 (Ω)	R2 (Ω)	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

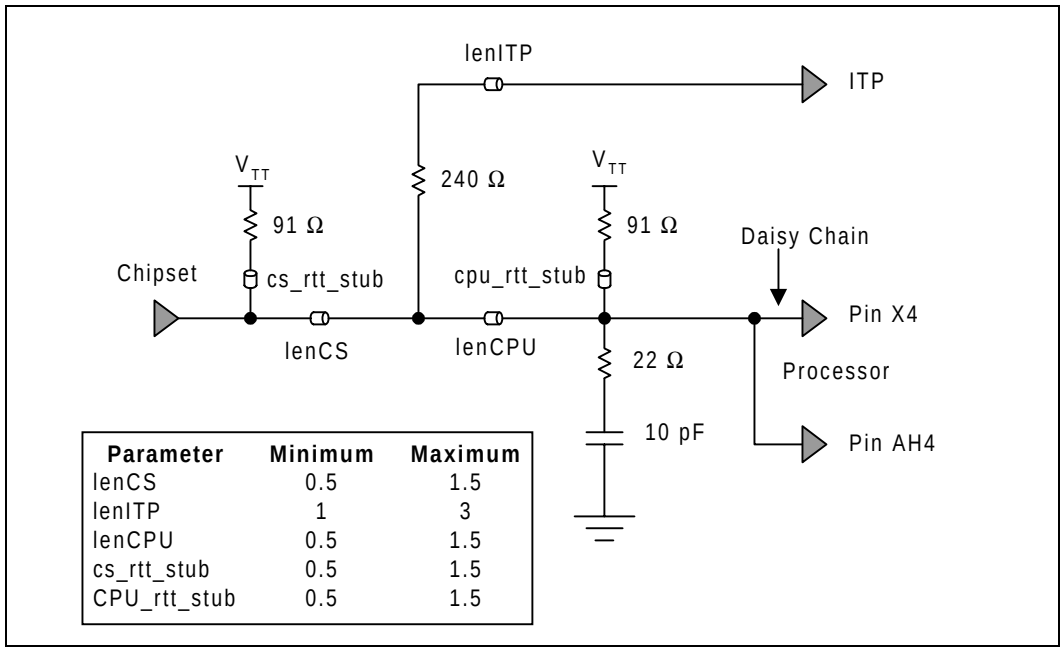
2.2.5 Undershoot/Overshoot Requirements

The Intel® Pentium® III processor has more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed a maximum absolute overshoot voltage limit (2.1V) and a minimum absolute undershoot voltage limit (-0.35V). Exceeding these limits will cause damage to the Intel® Pentium® III processor. There is also a time dependent, non-linear overshoot and undershoot requirement that is dependent on the amplitude and duration of the overshoot/undershoot. See the Intel® Pentium® III processor datasheet for more details on overshoot/undershoot specifications.

2.2.6 Connecting RESET# and RESET2# on a Flexible PGA370 Design

Intel® 810E chipset platform designs that support both the Intel® Celeron™ processor and Pentium® III processor mut route the AGTL+ reset signal from the chipset to two pins on the processor, as well as to the ITP connector. This reset segnal is conneted to pins AH4 (RESET#) and X4 (RESET#) at the PGA370 socket (see Figure 2-5).

Figure 2-5. RESET# Schematic for PGA370 Designs



Parameter	Minimum	Maximum
lenCS	0.5	1.5
lenITP	1	3
lenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
CPU_rtt_stub	0.5	1.5

On legacy Intel® 810 chipset platforms (ones that only have support for Intel® Celeron™ processors), RESET# is delivered only to pin X4. On Flexible Intel® 810E Chipset platforms (ones that have support for both Intel® Celeron™ processor and the Intel® Penitum® II processors) using a 370-pin socket, RESET# is delivered to both pins X4 *and* AH4.

2.2.7 Reset Strapping Options

LMD26 on the 82810E GMCH is used as a strap at reset to determine whether the system board is supporting a 370-pin socket or an SC242 connector:

LMD26: 0 or floating = 370-pin socket [leave as no connect]

1 = SC242 connector [pullup to 3.3V through an (approximately) 8.2KΩ pullup resistor]

2.2.8 Voltage Regulation Differences

The Intel® Pentium® III (FC-PGA w/256K L2 cache) processor requires the VRM or on-board voltage regulator to be compliant with Intel *VRM 8.4 DC-DC Converter Design Guidelines* revision 1.5 or greater. Important points to note regarding VRM 8.4 are:

- Intel® Celeron™ processor (PPGA) operates at VccCORE of 2.0V, Intel® Pentium® III- (FC-PGA w/128K L2 cache) operates at 1.5V, and Intel® Pentium® III-256K operates at 1.6V.
- Requirement for VRM 8.4 to support the Intel® Pentium® III processor at speeds greater than 650 MHz has changed from previous processors. Transient and static tolerances are tighter than VRM 8.2.
- Maximum current is increased to 18.4A for flexible motherboard designs.
- Additional motherboard decoupling required to meet VRM 8.4.

2.2.9 Decoupling Guidelines for Flexible PGA370 Designs

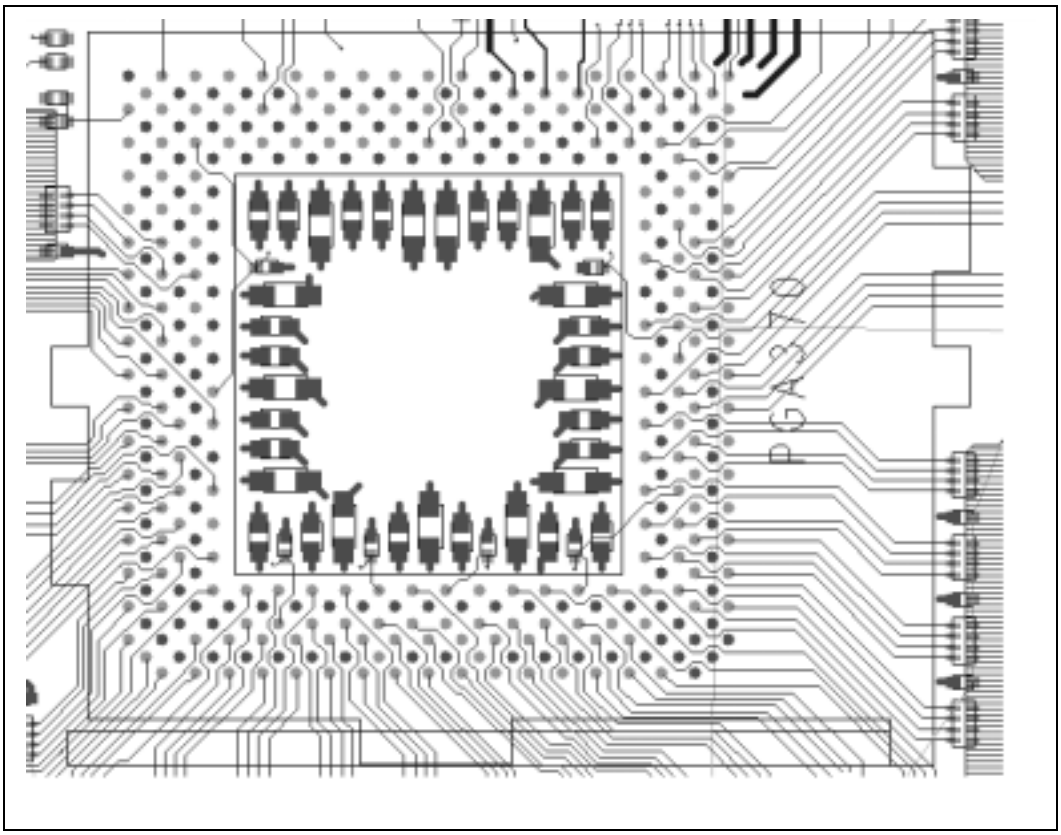
These are preliminary decoupling guidelines for *Flexible PGA370* designs and are estimated to meet VRM 8.4 V1.5 flexible motherboard guidelines (Vcc=1.6V, Icc = 0.8 - ~18.4A).

2.2.9.1 VCC_{CORE} Decoupling Design

- **Ten** or more 4.7 uF capacitors in 1206 packages.

  All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between VCC_{CORE}/Vss power pins, as shown in Figure 2-6.

Figure 2-6. Capacitor Placement on the Motherboard



2.2.9.2 Vtt Decoupling Design

For Itt = 3.0 A (max).

- ***Nineteen*** - 0.1 uF capacitors in 0603 packages placed within 200 mils of AGTL+ termination R-pack's, one capacitor for every two R-packs. These capacitors are shown on the outer exterior of Figure 2-6. These are located on the motherboard.

Vref Decoupling Design

- ***Four*** - 0.1uF capacitors in 0603 package placed near V_{REF} pins (within 500 mils).

2.2.10 Thermal/EMI Differences

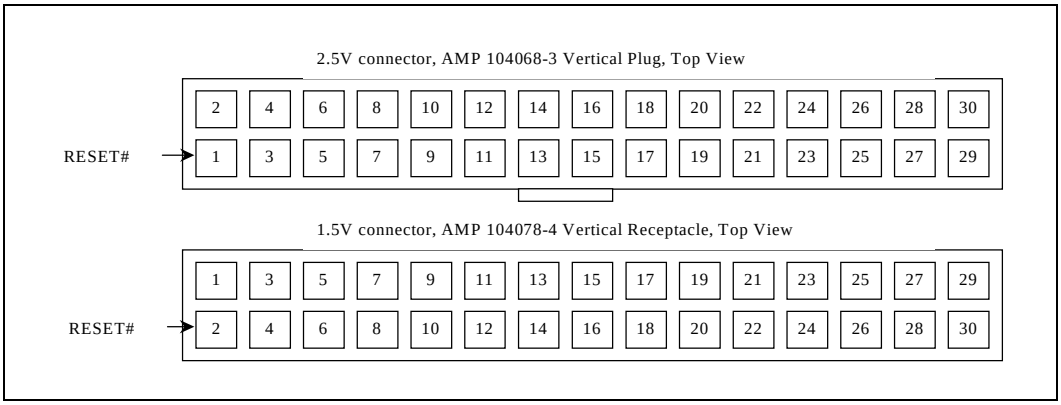
Heatsink requirements will be different for FC-PGA processors from previous processors using PPGA packaging. The current flexible motherboard guidelines for Intel® Pentium® III (FC-PGA w/256K L2 cache) processors calls for 28.4 W.

- Increased power density for Intel® Pentium® III processor (approximately 27 W/cm^2).
- Different thermal design verification for FC-PGA compared to PPGA packaged processors. Intel® Pentium® III processors are specified using Tjunction versus Tcase (used with Intel® Celeron™ processors).
- New heatsink for FC-PGA package which is not backwards compatible with PPGA processors.
- New heatsink clips for FC-PGA processor heatsinks.

2.2.11 Debug Port Changes

Due to the lower voltage technology employed with the Intel® Pentium® III processor, changes are required to support the debug port. Previously, the test access port (TAP) signals used 2.5V logic. This is the case with the Intel® Celeron™ processor in the PPGA package. Intel® Pentium® III utilizes 1.5V logic levels on the TAP. As a result, a new ITP connector is to be used on flexible PGA370 designs. The new 1.5V connector is the mirror image of the older 2.5V connector. Either connector will fit into the same printed circuit board layout. Just the pin numbers would change, as can be seen in the drawing below:

Figure 2-7. TAP Connector Comparison



Caution: The Intel® Pentium® III processor requires an in-target probe (ITP) with a 1.5V tolerant buffer. Previous ITPs are designed to work with higher voltages and may damage the processor if they are connected to an Intel® Pentium® III processor. See the Electrical, Mechanical and Thermal Specification EMTS) for more information regarding the debug port.



3

SC242 Processor Design Guidelines

SC242 Processor Design Guidelines 3

This chapter provides SC242 processor design guidelines including Layout Guidelines, general topology, minimizing crosstalk, motherboard layout rules for non-AGTL+ signals, THRMDP and THRMDN, and motherboard frequency select for SC242 designs. The layout guidelines are processor-specific and should be used in conjunction with the Chapter 4, "Layout and Routing Guidelines". See Chapter 5, "Advanced System Bus Design" for more details on AGTL+ layout guidelines.

3.1 Intel® Pentium® III Processors Layout Guidelines

The following layout guide supports designs using Intel® Pentium® III processors utilizing the SC242 connector and Intel® 810E chipset at system bus speeds of 100 MHz and 133 MHz.

Initial Timing Analysis

Table 3-1 lists the AGTL+ component timings of the processors and Intel® 810E GMCH defined at the pins. **These timings are for reference only; obtain each processor's specifications from its respective Electrical, Mechanical, and Thermal Specification and appropriate Intel® 810E chipset component specification.**

Table 3-1. Intel® Pentium® III Processor and Intel® 810E GMCH AGTL+ Parameters for Example Calculations[1]

IC Parameters	Intel® Pentium III processor core at 133 MHz System Bus	82810E GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	2.70	3.63	2
Clock to Output minimum (T_{CO_MIN})	-0.10	0.50	2
Setup time (T_{SU_MIN})	1.20	2.27	2,3
Hold time (T_{HOLD})	0.80	0.28	

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 2.72 ns assumes the 82810E GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 3-2 gives an example AGTL+ initial maximum flight time and Table 3-3 is an example minimum flight time calculation for a 133 MHz, uni-processor system using Intel® Pentium® III processor/Intel® 810E Chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

Table 3-2 and Table 3-3 are derived assuming:

- CLK_{SKEW} = 0.2 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.)
- CLK_{JITTER} = 0.250 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the respective processor's Electrical, Mechanical, and Thermal Specification, appropriate Intel® 810E Chipset documentation, and *CK810E Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications.

Table 3-2. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	82810E GMCH	7.50	2.70	2.27	0.20	0.25	0.40	1.68
82810E GMCH	Processor	7.50	3.63	1.20	0.20	0.25	0.40	1.82

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   - The effective board propagation constant (S_{EFF}), which is a function of:
     — Dielectric constant (ε_r) of the PCB material.
     — The type of trace connecting the components (stripline or microstrip).
     — The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

Table 3-3. Example T_{FLT_MIN} Calculations (Frequency Independent)[1]

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	82810E GMCH	0.28	0.20	-0.10	0.58
810E GMCH	Processor	0.80	0.20	0.50	0.50

NOTES:
1. All times in nanoseconds.

3.2 Determine General Topology and Layout

Figure 3-1 provides segment descriptions and length recommendations for the investigated topology shown. Segment lengths are defined at the pins of the devices or components. To ensure processor signal integrity requirements, **it is highly recommended that all system bus signal segments to be referenced to the ground plane for the entire route.**

Figure 3-1. Intel® Pentium® III Uni-Processor Configuration

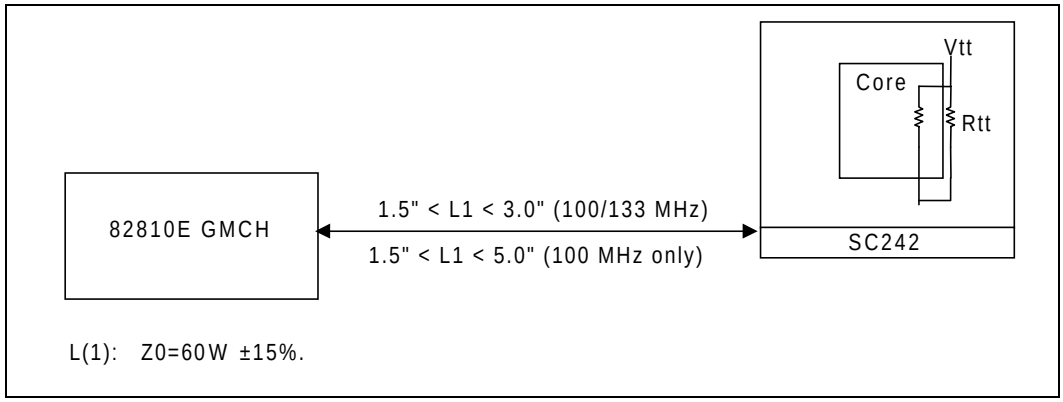


Table 3-4. Segment Descriptions and Lengths for Figure 3-2 [1]

Segment	Description	Min length (inches)	Max length (inches)
L1 (100/133 MHz)	GMCH to SC242	1.50	3.00
L1 (100 MHz only)	GMCH to SC242	1.50	5.00

NOTE: 1 - All AGTL+ bus signals should be referenced to the ground plane for the entire route.

3.3 Solution Space

- AGTL+ signals should be routed with trace lengths within the range specified for L1 from the processor pin to the chipset.
- Use an intragroup AGTL+ spacing to line width to dielectric thickness ratio of at least 2:1:1 for microstrip geomety. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
- The trace width is recommended to be 5 mils and not greater than 6 mils.

Table 3-5 contains the trace width:space ratios assumed for this topology. The crosstalk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intragroup AGTL+ crosstalk involves interference between AGTL+ signals within the same group. Intergroup AGTL+ crosstalk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ crosstalk is when CMOS and AGTL+ signals interfere with each other.

Table 3-5. Trace Width:Space Guidelines

Crosstalk Type	Trace Width:Space Ratios
Intragroup AGTL+ signals (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ signals (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

3.4 Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.
- For the clock trace, provide a guard ground trace or spacing of at least about 25 mils to the edge of the adjacent trace.

3.5 Motherboard Layout Rules for Non-AGTL+ (CMOS) Signals

Non-AGTL+ (CMOS) Signals

Route these signals on any layer or any combination of layers.

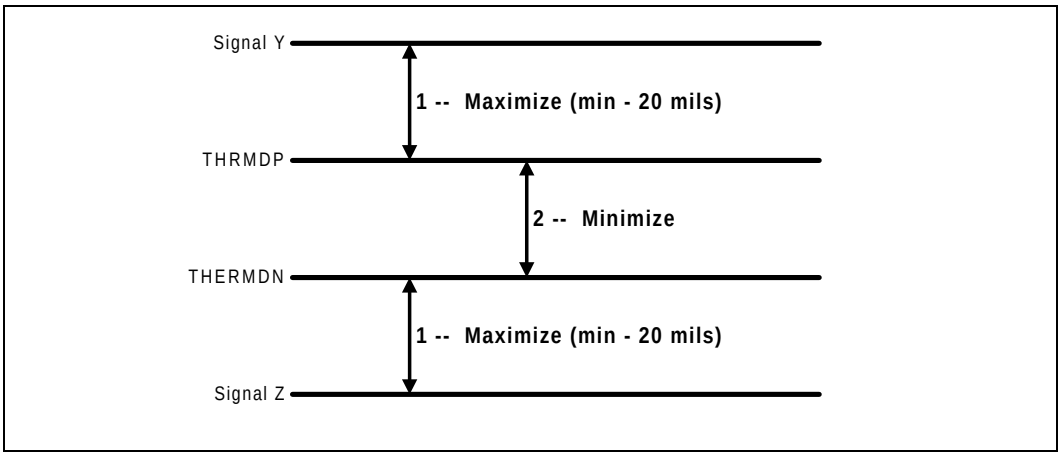
Table 3-6. Routing Guidelines for Non-AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 6”
FERR#	5 mils	10 mils	1” to 6”
FLUSH#	5 mils	10 mils	1” to 6”
IERR#	5 mils	10 mils	1” to 6”
IGNNE#	5 mils	10 mils	1” to 6”
INIT#	5 mils	10 mils	1” to 6”
THERMTRIP#	5 mils	10 mils	1” to 6”
LINT[0] (INTR)	5 mils	10 mils	1” to 6”
LINT[1] (NMI)	5 mils	10 mils	1” to 6”
PWRGOOD	5 mils	10 mils	1” to 6”
SLP#	5 mils	10 mils	1” to 6”
PICD[1:0]	5 mils	10 mils	1” to 8”
PREQ#	5 mils	10 mils	1” to 6”
SMI	5 mils	10 mils	1” to 6”
STPCLK#	5 mils	10 mils	1” to 6”

3.6 THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor's thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance. Refer to Figure 3-2.

Figure 3-2. Routing for THRMDP and THRMDN



Rule

Length Equalization	route these traces parallel ±0.5"
Layer	route both on the same layer

3.7 Additional Considerations

- Distribute Vtt with a wide trace. A 0.050" minimum trace is recommended to minimize DC losses. Route the Vtt trace to all components on the host bus. Be sure to include decoupling capacitors. Guidelines for Vtt distribution and decoupling are contained in *AP-907: Pentium® III Processor Power Distribution Guidelines, Order # 245085.*
- The Vtt voltage should be 1.5V ±3% for static conditions, and 1.5V ±9% for transient condition.
- Place resistor divider pairs for V_{REF} generation at the 82810E GMCH component. No V_{REF} generation is needed at the processor. V_{REF} is generated locally on the processor. Be sure to include decoupling capacitors. Guidelines for V_{REF} distribution and decoupling are contained in *AP-907: Pentium® III Processor Power Distribution Guidelines (Order # 245085).*

3.8 Motherboard Frequency Select for SC242 Designs

Figure 3-3 shows the 82810E GMCH and Processor straps for selecting the system bus frequency.

Figure 3-3. System Bus Frequency Selection Topology for SC242

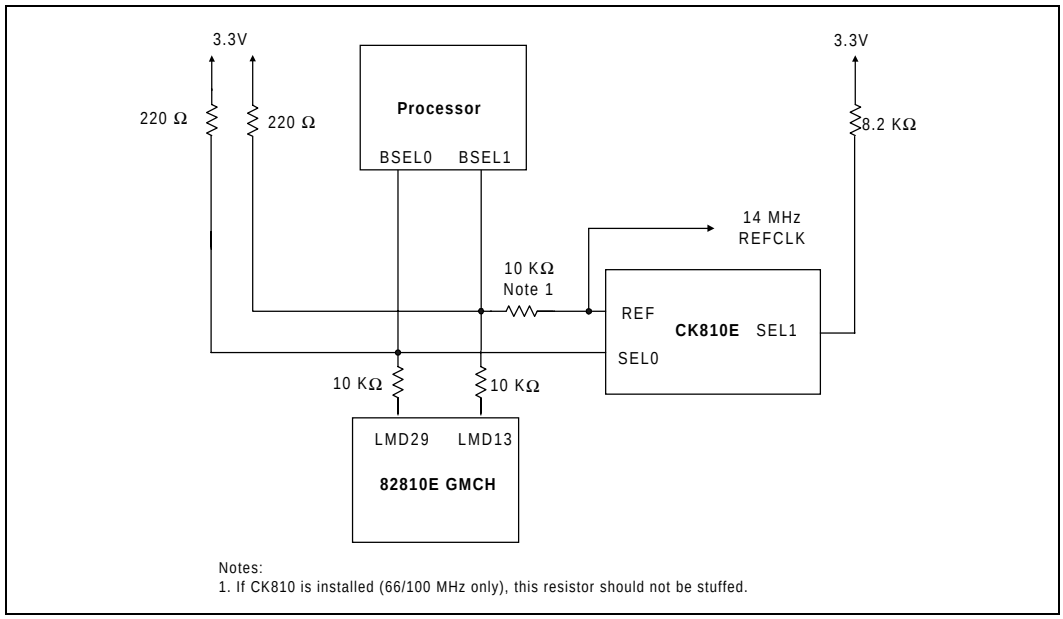


Table 3-7 shows the 82810E Reset Strapping matrix.

Table 3-7. 82810E Reset Strapping Matrix

REF	SEL1	SEL0	CK810E Function
X	0	0	Tristate
X	0	1	Test
0	1	0	Active CPU = 66 MHz
0	1	1	Active CPU = 100 MHz
1	1	1	Active CPU = 133 MHz
1	1	0	Reserved

3.9 S.E.C.C. 2 Grounding Retention Mechanism (GRM)

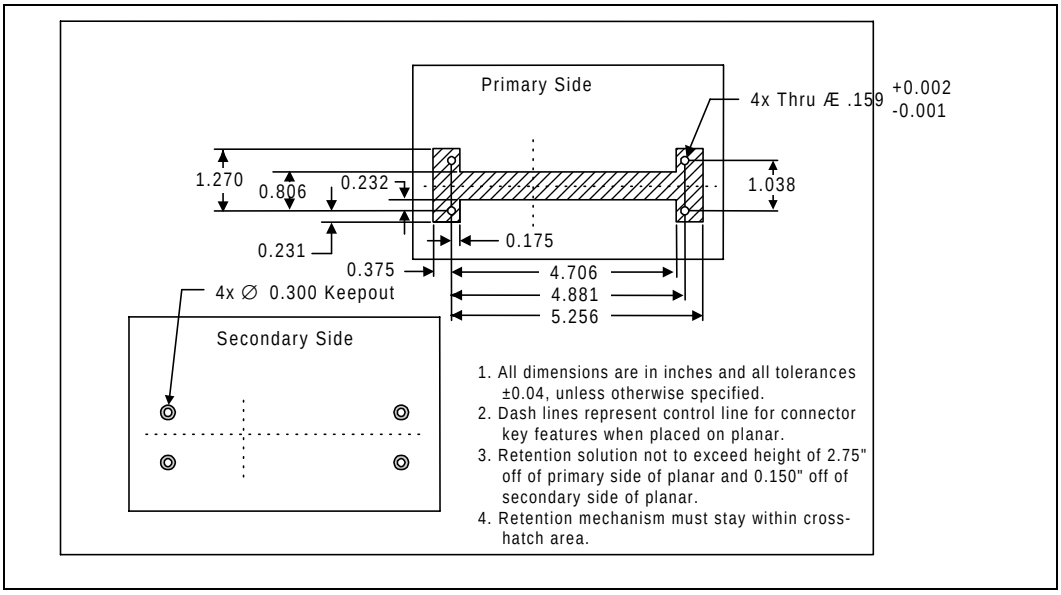
Intel is enabling a new S.E.P.P. (Single Edge Processor Package) style retention mechanism which will provide a grounding path for the heatsink on processors in the S.E.C.C. 2 (Single Edge Contact Cartridge) package. This solution is referred to as the S.E.C.C.2 Grounding Retention Mechanism (GRM). OEMs who choose to utilize this new solution will need to add grounding pads on the primary side of the motherboard which will interface with the enabled GRM. If the motherboard or heat sink do not have the proper interfaces, then the GRM may not be utilized to its full ability, and/or damage could occur to the motherboard.

The most notable interface requirement to accommodate the GRM is the addition of grounding pads around two of the Retention Mechanism (RM) mounting holes within the existing RM keep-out zone on the motherboard. The other interface is a contact area on the heat sink flanges. The interface size and locations for the motherboard are discussed in detail further in this section.

The reference design GRM is asymmetric, and requires 0.159” mounting holes. To minimize the impact to trace routing, only two ground pads are required. This makes it necessary to key the GRM to prevent the ground clips from being installed on soldermask instead of the grounding pads. This keying is accomplished by making the GRM asymmetric. The requirement for the 0.159” mounting holes is for the supported plastic fastener attachment mechanism.

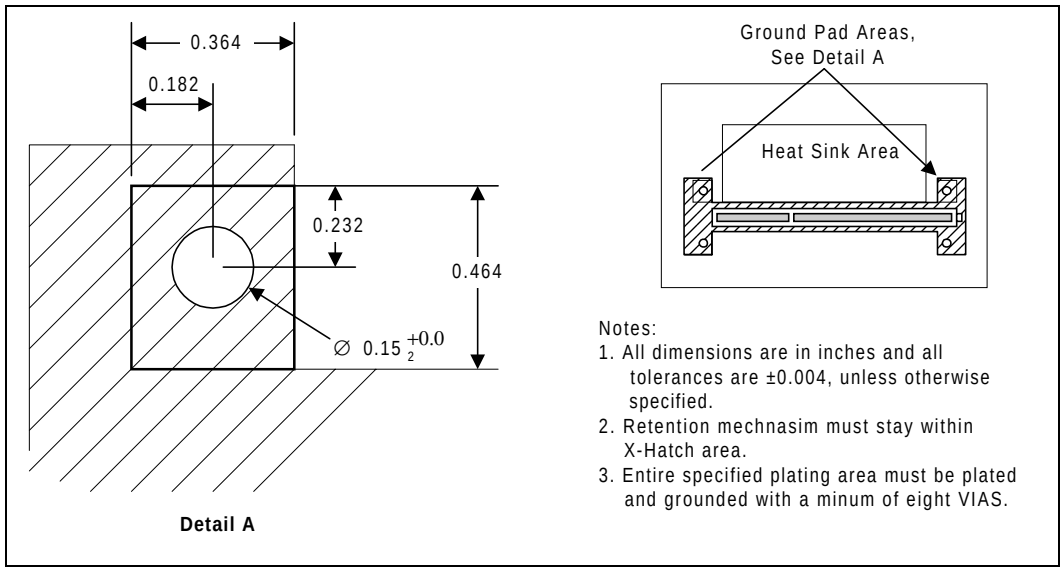
3.9.1 Motherboard Interfaces

Figure 3-4. Hole Locations and Keep-out Zones for Support Components



NOTES:
1. Hole Locations and Keep-out Zones are from the motherboard surface to .100” above the motherboard surface.)
2. The dashed lines represent the centerlines for the connector keying features.

Figure 3-5. Detailed Drawing of Minimum Ground Pad Size and Location



NOTE: NOTE: DRAWING NOT TO SCALE

It is not recommended to use the GRM without the minimum size ground pads in the correct locations. If the GRM is used without the correct pads, then there is a high risk that the metal clip that grounds to the motherboard will be touching the solder mask on the top layer of the board, and possibly short out traces immediately beneath the solder mask, resulting in board failure. The required thickness of the pad is less than 0.001” (using 1/2 oz copper).



4

Layout and Routing Guidelines

Layout and Routing Guidelines 4

This chapter describes motherboard layout and routing guidelines for Intel® 810E Chipset systems, except for the processor layout guidelines. For the PGA370 processor specific layout guidelines, refer to Chapter 2, "PGA370 Processor Design Guidelines". For the SC242 processor specific layout guidelines, refer to Chapter 3, "SC242 Processor Design Guidelines". This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

Note: **If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.** Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines should be simulated.

4.1 General Recommendations

The trace impedance typically noted (i.e., 60 ohm ±15%) is the "nominal" trace impedance for a 5 mil wide trace (i.e., the impedance of the trace when not subjected to the fields created by changing current in neighboring traces). When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

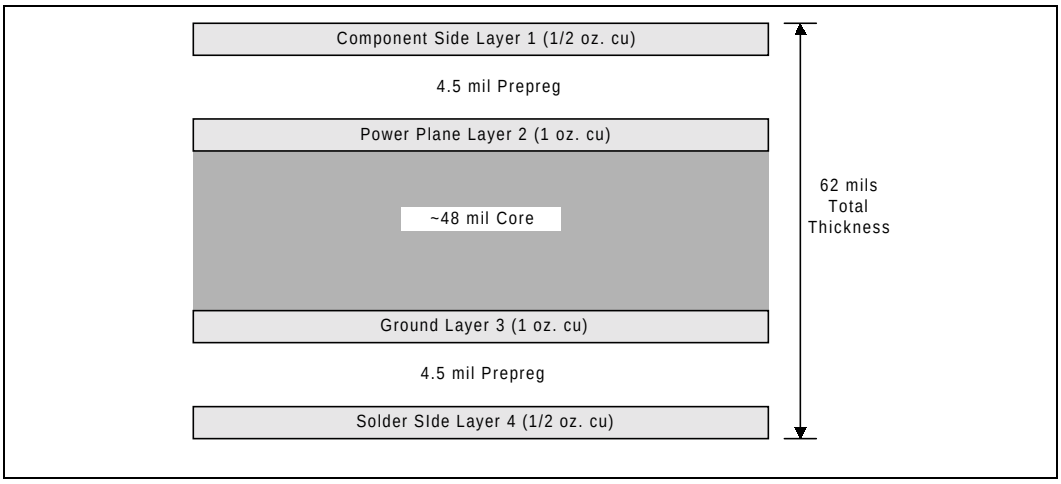
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using the *stack-up* (refer to Figure 4-1). If this stack-up is not used, simulations should be completed.

4.2 Nominal Board Stackup

The Intel® 810E Chipset platform requires a board stackup yielding a target impedance of 60 ohm ±15% with a 5 mil nominal trace width. Figure 4-1 presents an example stackup to achieve this. It is a 4-layer fabrication construction using 53% resin, FR4 material.

Figure 4-1. Nominal Board Stackup



4.3 Component Quadrant Layouts

Figure 4-2. GMCH Quadrant Layout (topview)

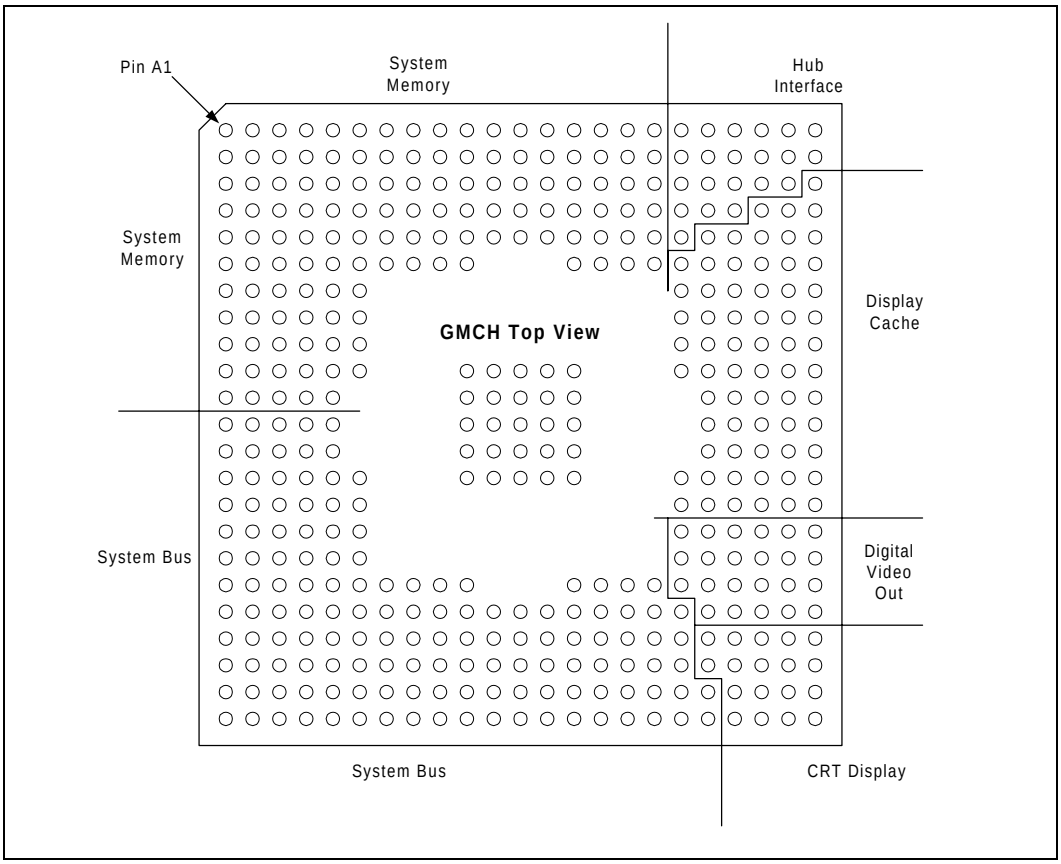
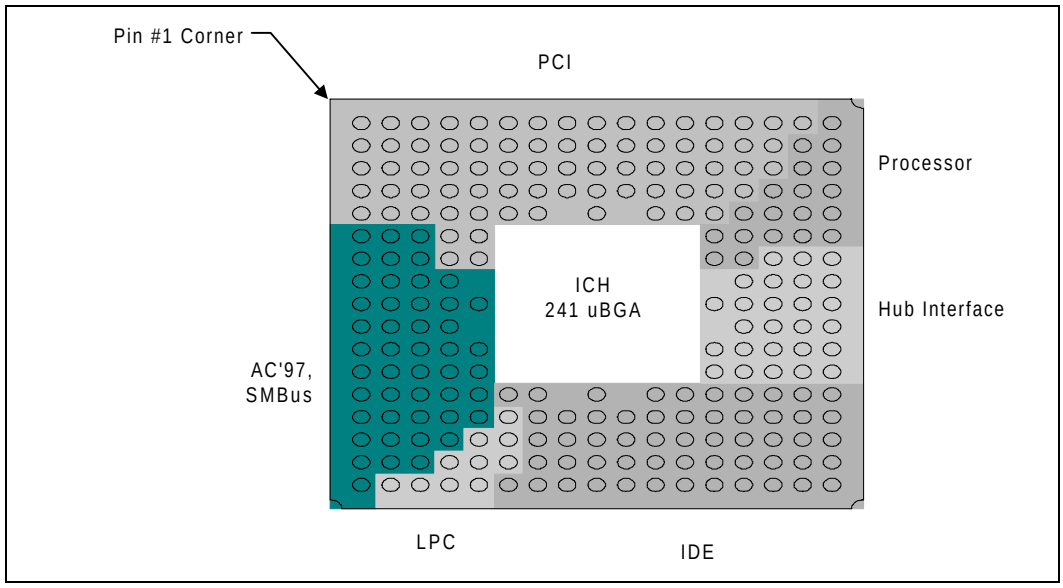


Figure 4-3. ICH 241-uBGA Quadrant Layout (topview)

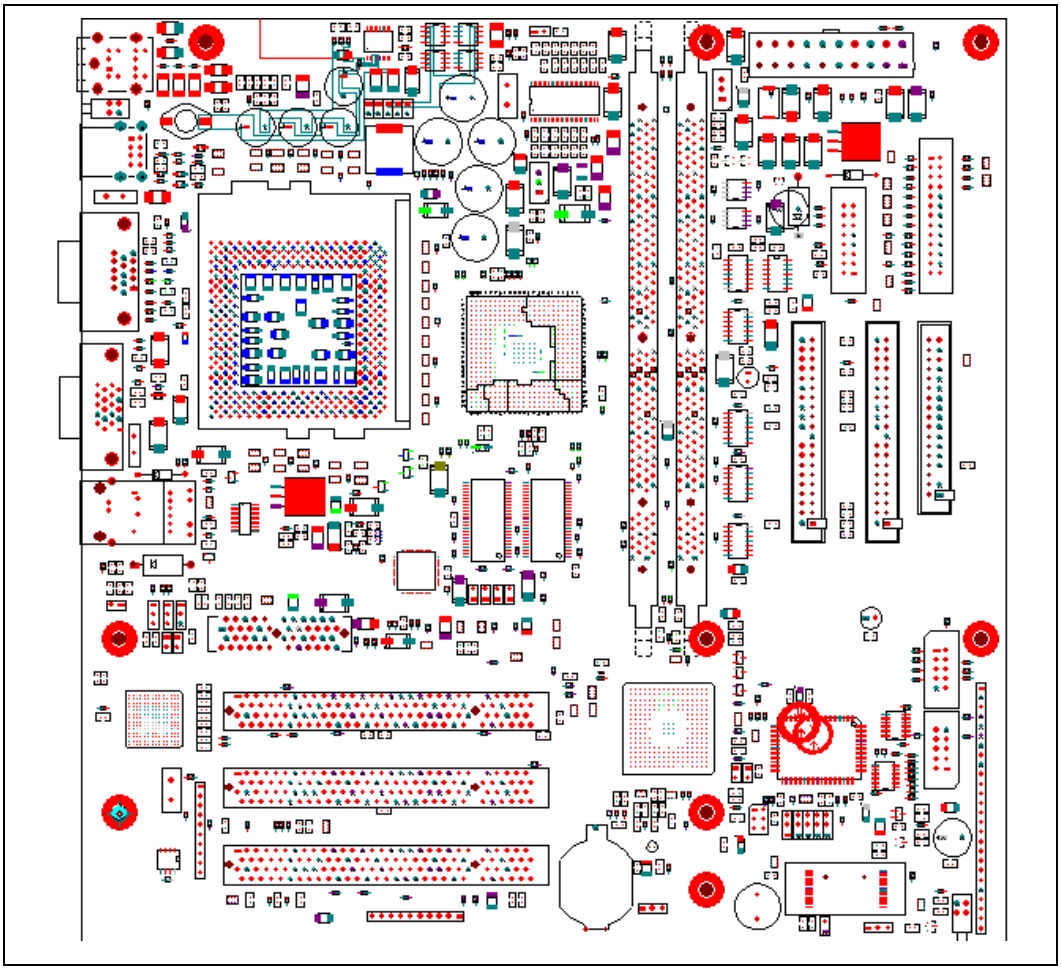


4.4 Intel® 810E Chipset Component Placement

The assumptions for component placement are:

- uATX Form Factor
- 4-Layer Motherboard
- Single Sided Assembly

Figure 4-4. uATX Placement Example for PGA370 Processors



4.5 System Memory Layout Guidelines

4.5.1 System Memory Solution Space

Figure 4-5. System Memory Topologies

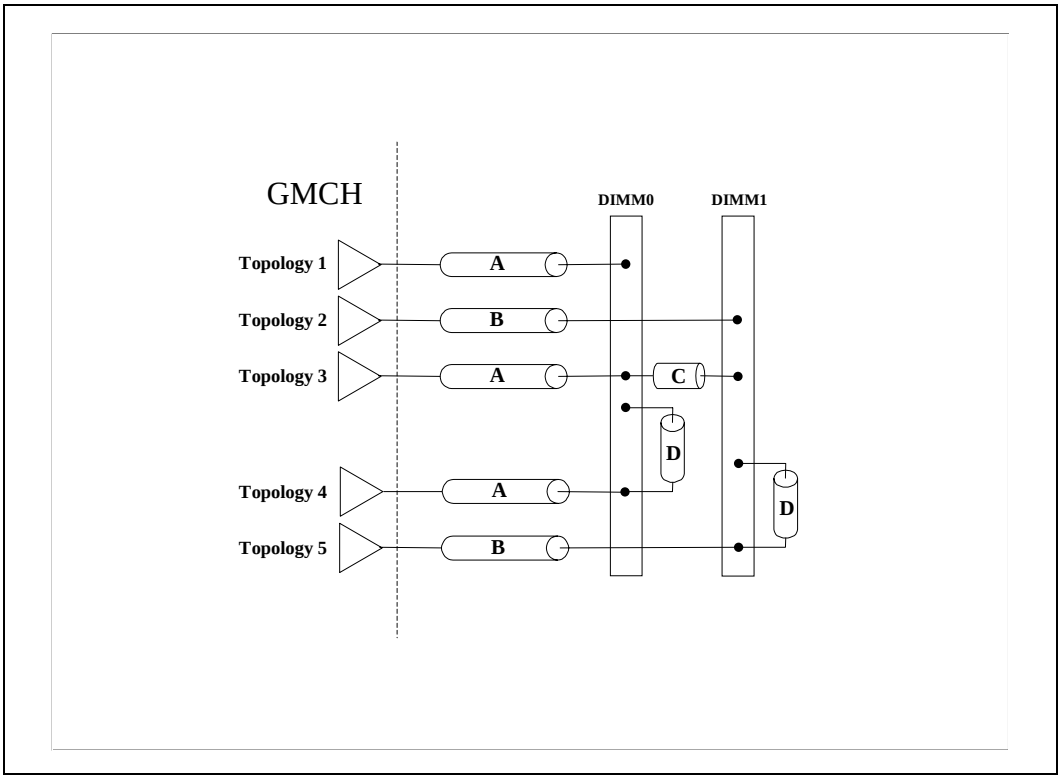


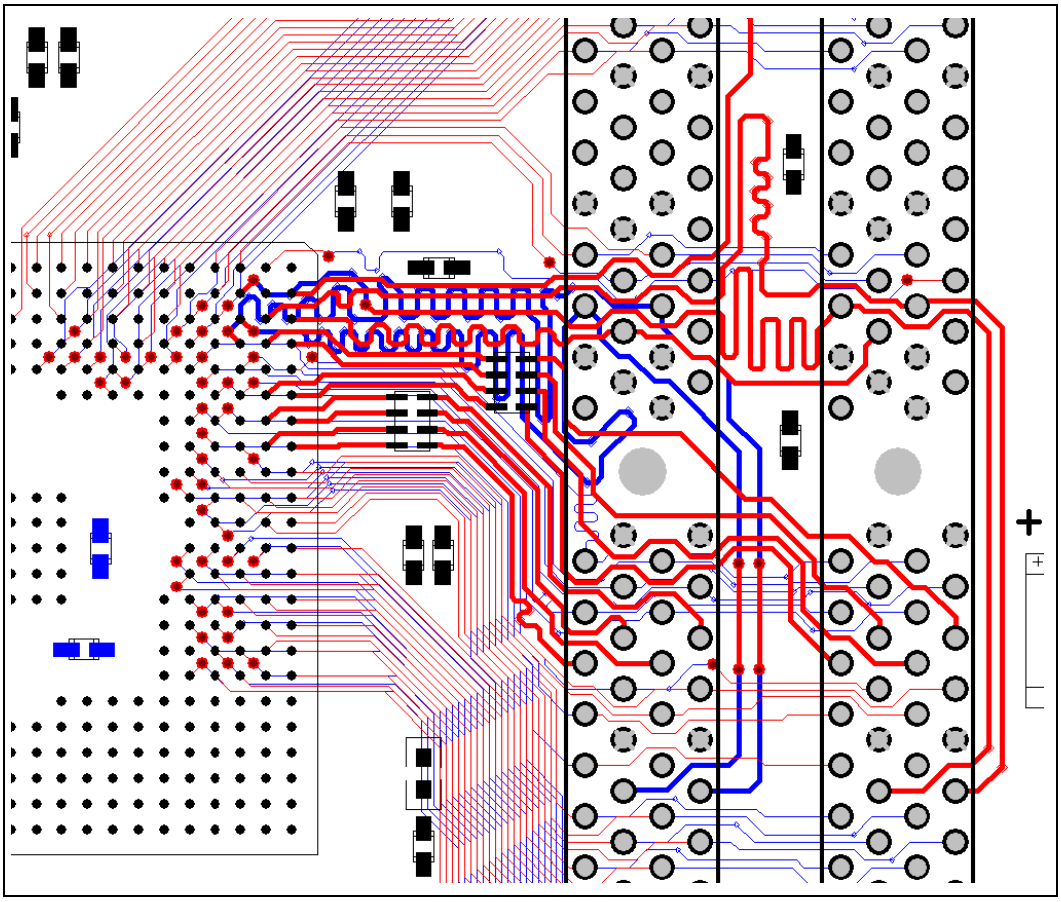
Table 4-1. System Memory Routing

Signal		Top.	Trace (mils)		Trace Lengths (inches)												
					A	B		C		D		E		F		G	
			Width	Space	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCS[3:2]#	Opt.1	5	10	8								3	5			1.5	2
	Opt.2	5	10	8								2.2	5			1.5	1.8
	Opt.3	5	10	8								1.6	5			1.15	1.5
SCS[1:0]#	Opt.1	4	10	8						3	5					1.5	2
	Opt.2	4	10	8						2.2	5					1.5	1.8
	Opt.3	4	10	8						1.6	5					1.15	1.5
SMAA[7:4]		1	10	8	0.5	0.5	2										
SMAB[7:4]#		2	10	8	0.5			0.5	2								
SCKE[1:0]		3	10	8						1	2.5			0.4	1		
SMD[63:0], SDQM[7:0]		3	5	7						1	3			0.4	1		
SCAS#, SRAS#, SWE#		3	5	7						1	3.5			0.4	1		
SBS[1:0], SMAA[11:8, 3:0]		3	5	7						1	2.5			0.4	1		

NOTE: It is recommended to add 10 ohm series resistors to the MAA[7:4] and the MAB[7:4] lines as close as possible to GMCH for signal integrity.

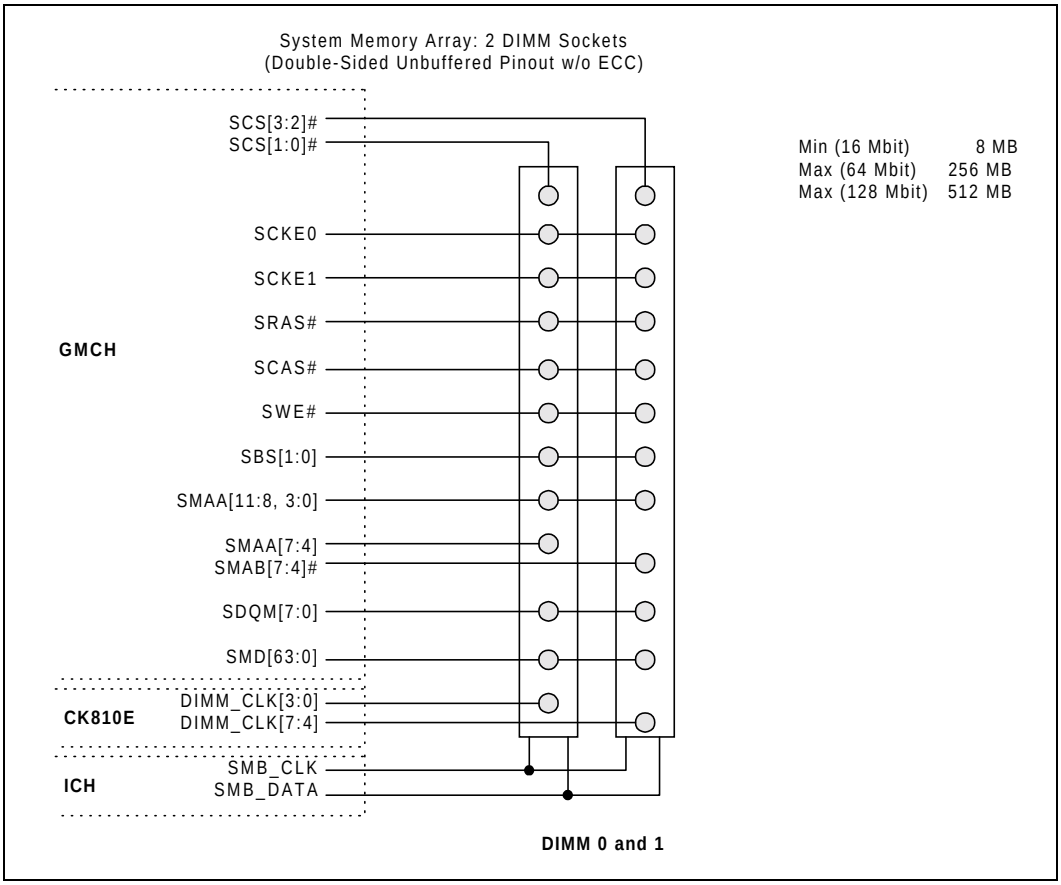
4.5.2 System Memory Routing Example

Figure 4-6. System Memory Routing Example



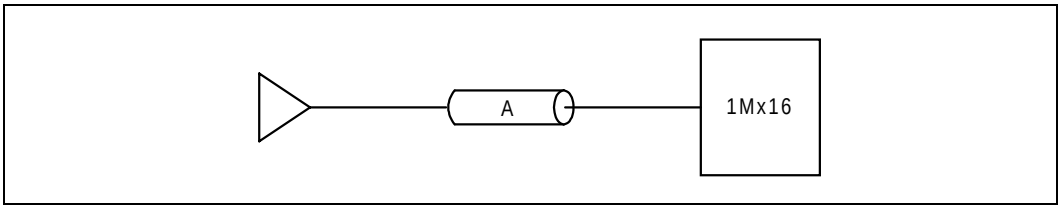
4.5.3 System Memory Connectivity

Figure 4-7. System Memory Connectivity



4.6 Display Cache Interface

Figure 4-8. Display Cache (Topology 1)



4.6.1 Display Cache Solution Space

Table 4-2. Display Cache Routing (Topology 1)

Signal	Topology	Trace (mils)		A (inches)	
		Width	Spacing	Min	Max
LMD[31:0], LDQM[3:0]	1	5	7	1	5

NOTE: Trace Length (inches)

Figure 4-9. Display Cache (Topology 2)

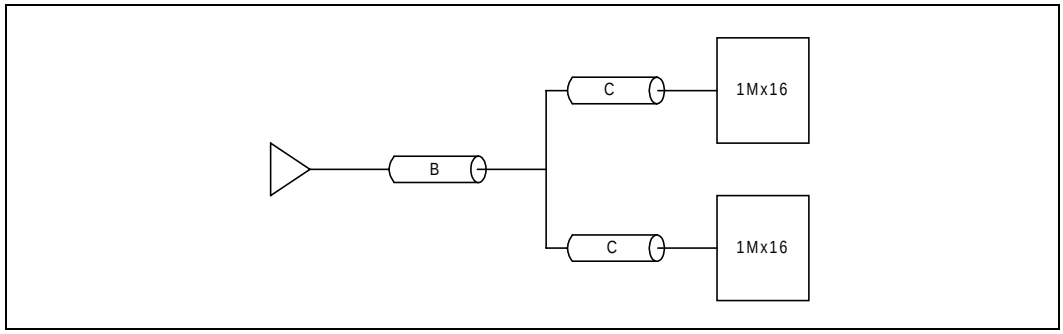


Table 4-3. Display Cache Routing (Topology 2)

Signal	Topology	Trace (units=mils)		B (inches)		C (inches)	
		Width	Spacing	Min	Max	Min	Max
LMA[11:0], LWE#, LCS#, LRAS#, LCAS#	2	5	7	1	3.75	0.75	1.25

Figure 4-10. Display Cache (Topology 3)

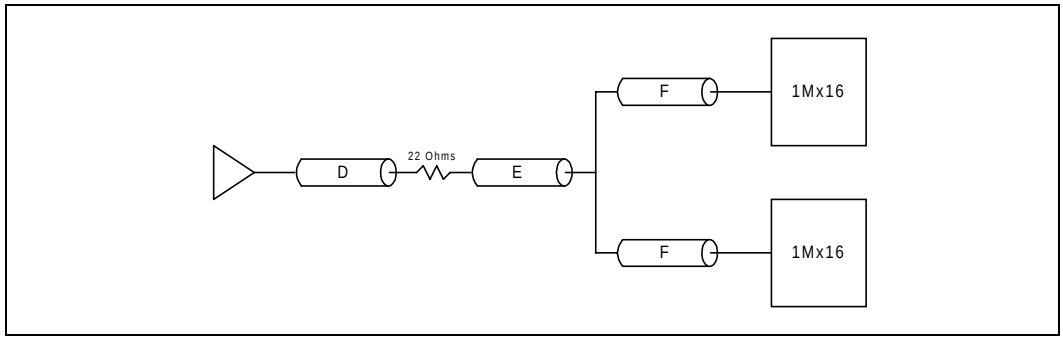


Table 4-4. Display Cache Routing (Topology 3)

Signal	Topology	Trace (units=mils)		D (inches)	E (inches)		F (inches)	
		Width	Spacing	Length	Min	Max	Min	Max
TCLK	3	5	7	0.5	1.5	2.5	0.75	1.25

Figure 4-11. Display Cache (Topology 4)

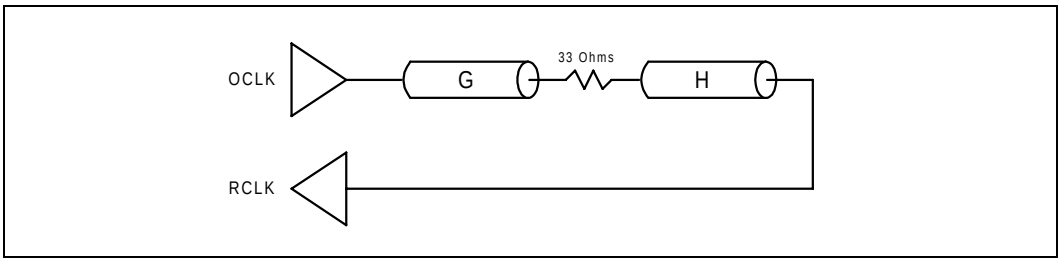


Table 4-5. Display Cache Routing (Topology 4)

Signal	Topology	Trace (units=mils)		G (inches)	H (inches)	
		Width	Spacing	Length	Min	Max
OCLK	4	5	6	0.5	3.25	3.75

4.7 Hub Interface

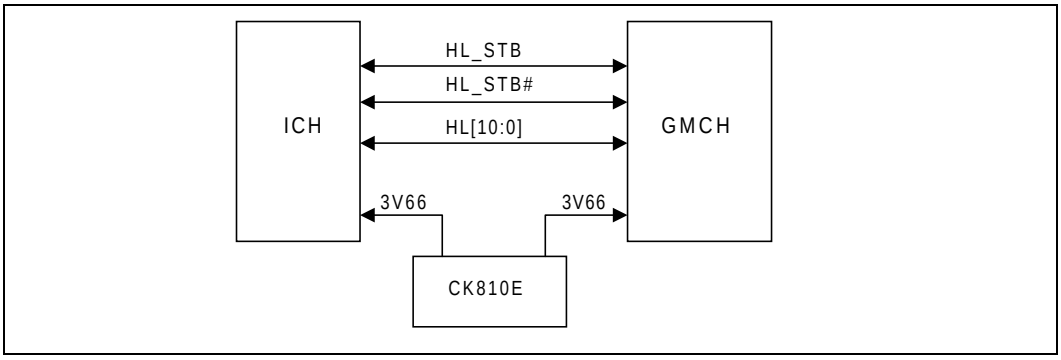
The GMCH ball assignment and ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals are routed directly from the GMCH to the ICH on the top signal layer (refer to Figure 4-12). The hub interface has two signal groups:

- Data Signals: HL[10:0]
- Strobe Signals: HL_STB, HL_STB# (differential strobe pair).

There are no pull-ups or pull-downs required on the hub interface. HL11 can be brought out to a test point for NAND Tree testing.

Each signal should be routed such that the signal meets the guidelines documented for its signal group.

Figure 4-12. Hub Interface Signal Routing Example



4.7.1 Data Signals

Hub interface data signals should be routed with a trace width of *5* mils and a trace spacing of *20* mils. These signals can be routed with a trace width of *5* mils and a trace spacing of *15* mils for navigation around components or mounting holes. To break-out of the GMCH and the ICH, the hub interface data signals can be routed with a trace width of *5* mils and a trace spacing of *5* mils. The signals should be separated to a trace width of *5* mils and a trace spacing of 20 mils within 0.3" of the GMCH/ICH components.

The maximum trace length for the hub interface data signals is 7". These signals should each be matched within ±0.1" of the HL_STB and HL_STB# signals.

4.7.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7" and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes with ±0.1".

4.7.3 HREF Generation/Distribution

HREF is the hub interface reference voltage. It is 0.5 * 1.8V = 0.9V ±2%. It can be generated locally, or a single HREF divider can be used (as shown in Figure 4-13 and Figure 4-14). Each divider consists of a DC element and an AC element. The resistors in the DC element should be equal in value and rated at 1% tolerance. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The resistors in the AC element of the resistor divider should be no greater than 80 ohm and the capacitors should be 500 pF. Additionally, the reference voltage should be bypassed to ground at each component with a 0.1 uF capacitor.

Figure 4-13. Single Hub Interface Reference Divider Circuit

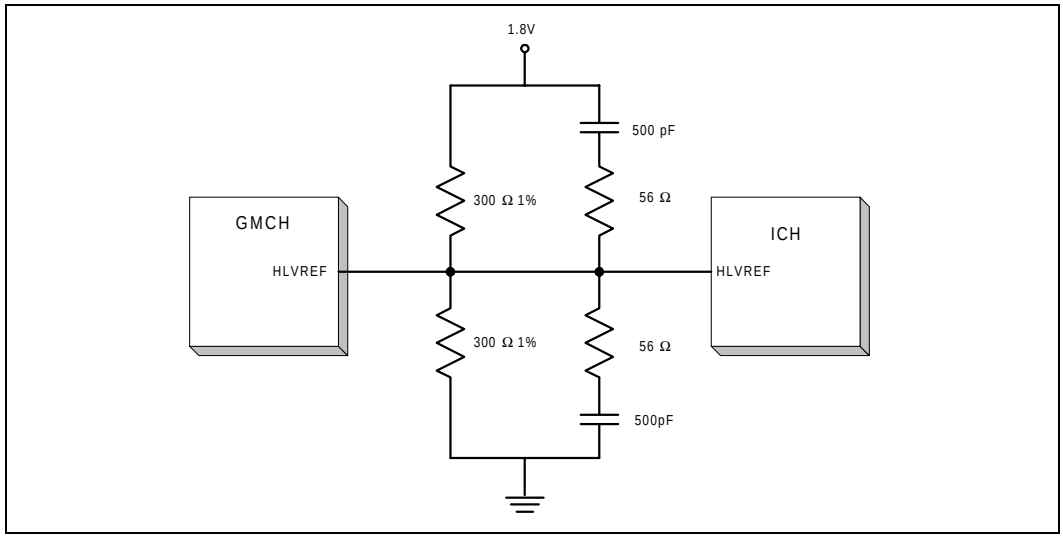
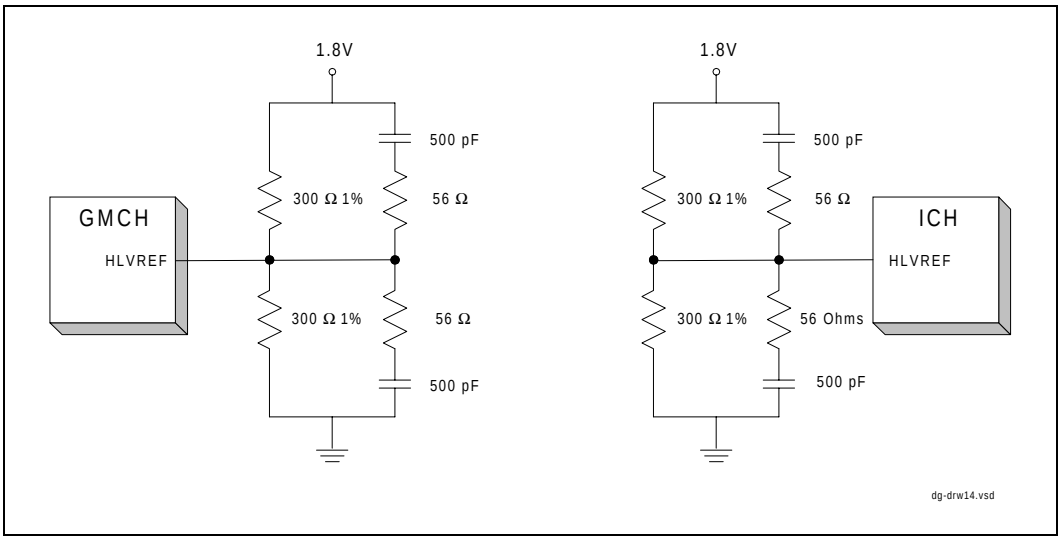


Figure 4-14. Locally Generated Hub Interface Reference Dividers



4.7.4 Compensation

There are two options for the ICH hub interface compensation (HLCOMP). HLCOMP is used by the ICH to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet for details on compensation. It can be used as either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP). The guidelines are below:

- **RCOMP:** Tie the HLCOMP pin to a 40 ohm 1% or 2% pull-up resistor (to 1.8V) via a 10 mil wide, 0.5” trace (targeted for a nominal trace impedance of 40 ohm).
- **ZCOMP:** The HLCOMP pin should be tied to a 10 mil trace that is AT LEAST 18” long. This trace should be unterminated and care should be taken when routing the signal to avoid crosstalk (15-20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

The GMCH also has a hub interface compensation pin. This signal (HLCOMP) can be routed using either the RCOMP method or ZCOMP method described for the ICH.

4.8 Ultra ATA/66

4.8.1 IDE Routing Guidelines

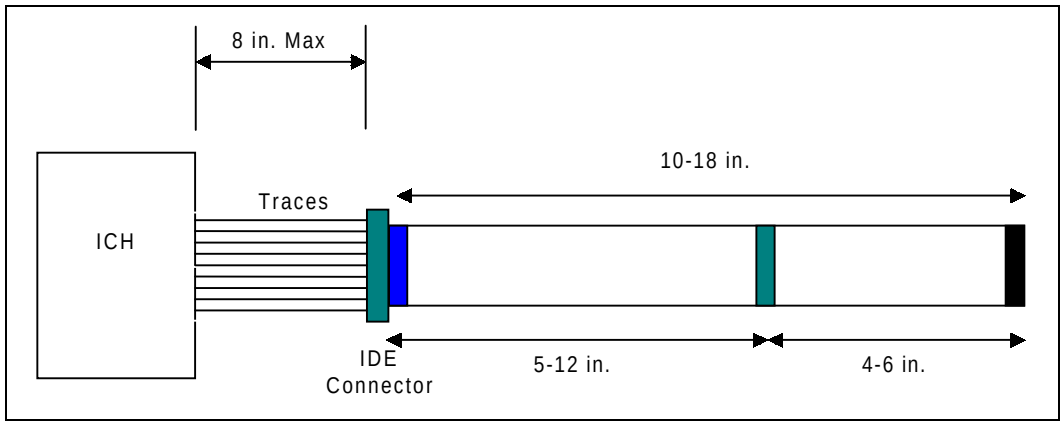
This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH0 and the ICH has integrated the series terminating resistors that have been typically required on the IDE data and control signals running to the two ATA connectors.

The IDE interface can be routed with 5 mil traces on 5 mil spaces and should be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 1” shorter than the longest IDE signal (on the channel).

Cabling

- **Length of Cable:** Each IDE cable should be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **UltraATA/66:** Ultra ATA/66 requires the use of an 80 conductor cable
- **ICH Placement:** The ICH should be placed within 8” of the ATA connector.
- **PC99 Requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC99. The CSEL signal needs to be pulled down at the host side by using a 470 ohm pull-down resistor for each ATA connector.

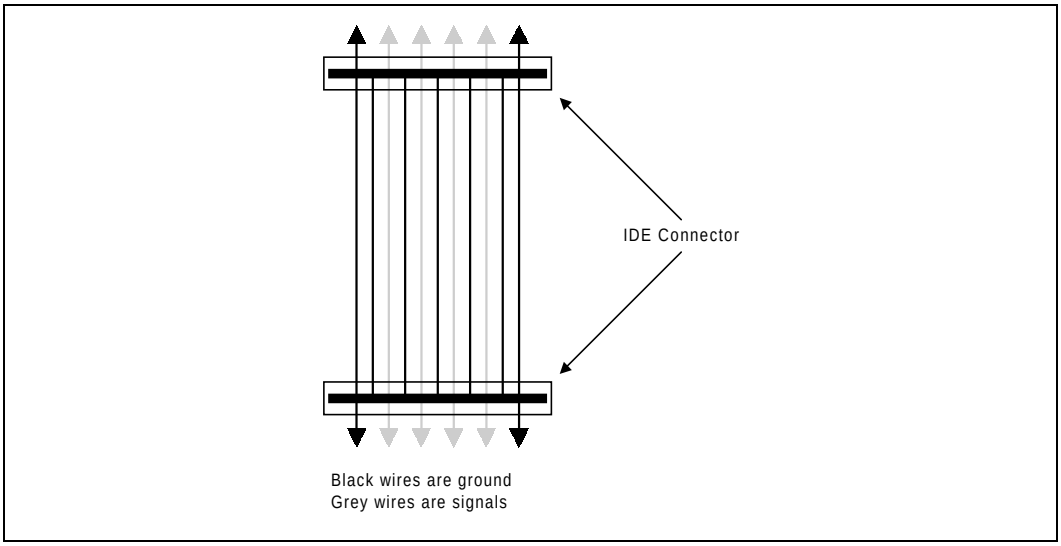
Figure 4-15. IDE Min/Max Routing and Cable Lengths



A new IDE cable is required for Ultra ATA/66. This cable is an 80 conductor cable; however, the 40 pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to

the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

Figure 4-16. Ultra ATA/66 Cable



Motherboard

- **ICH Placement:** The ICH should be placed within 8” of the ATA connector(s). There are no minimum length requirements for this spacing.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- **Series Termination:** There is no need for series termination resistors on the data and control signals since there is series termination integrated into these signal lines on the ICH.
  - A 1K ohm pullup to 5V is required on PIORDY and SIORDY.
  - A 470 ohm pulldown is required on pin 28 of each connector.
  - A 5.6K ohm pulldown is required on PDREQ and SDREQ.
  - Support Cable Select (CSEL) is a PC99 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
  - Primary IDE connector uses IRQ14 and the secondary IDE connector uses IRQ15.
  - IRQ14 and IRQ15 each need an 8.2K ohm pull-up resistor to VCC.
  - Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Due to high loading, the PCI_RST# signal should be buffered.
  - There is no internal pull up or down on PDD7 or SDD7 of the ICH. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10K ohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).
  - If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals left as no connects.

Figure 4-17. Resistor Schematic for Primary IDE Connectors

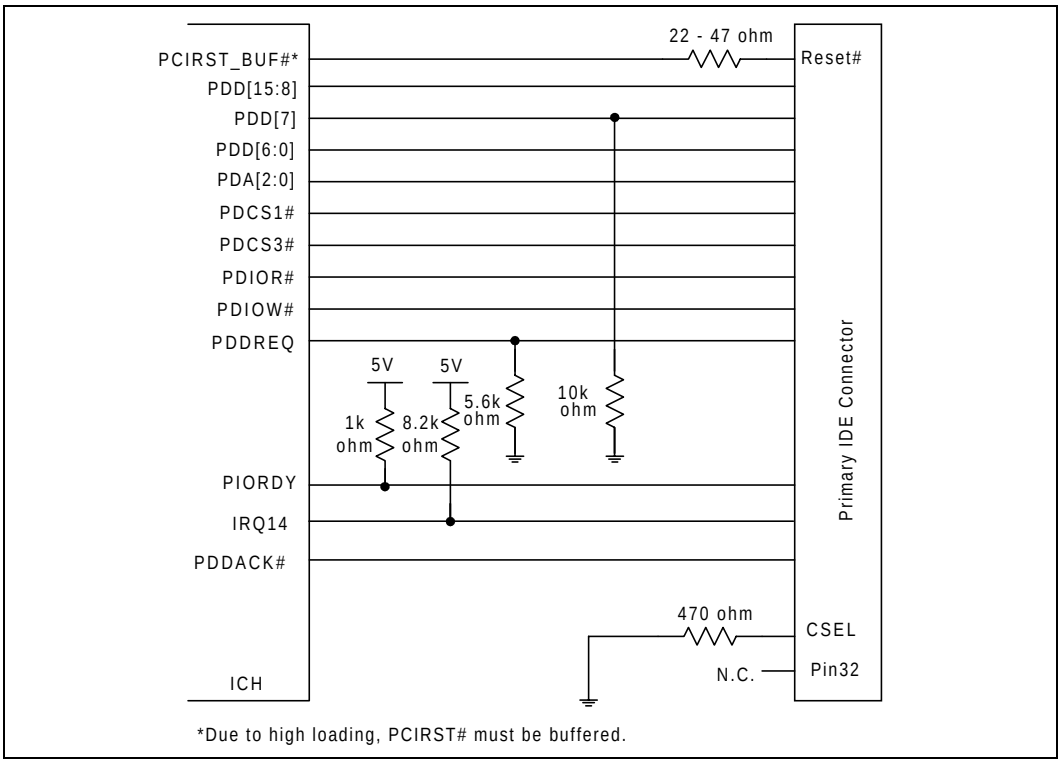
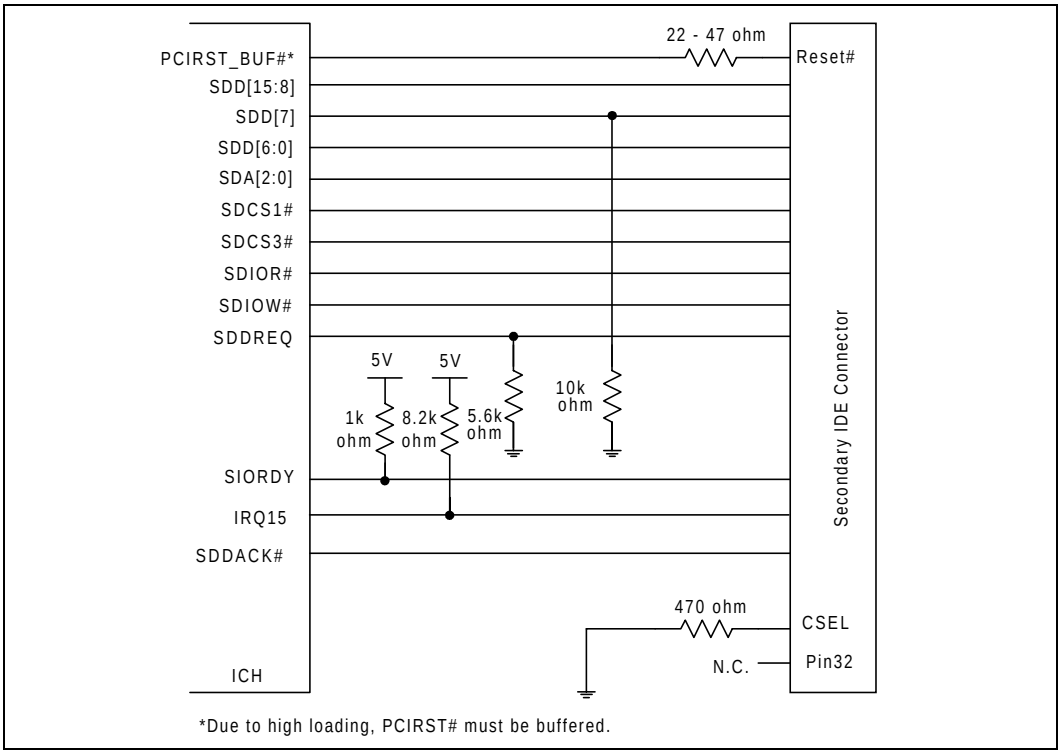


Figure 4-18. Resistor Schematic for Secondary IDE Connectors



4.8.2 Ultra ATA/66 Detection

The 82801AA ICH supports Ultra ATA/66 devices. The ATA/66 cable is an 80-conductor cable; however the 40 pin connectors used on motherboards for 40-conductor cables do not change as a result of this new cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together at the connectors on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

To determine if ATA/66 mode can be enabled, the Intel® 810E Chipset using the ICH requires the system BIOS to attempt to determine the cable type used in the system. The BIOS does this in one of two ways:

- Host Side Detection
- Device Side Detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (example: Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS will configure the Intel® 810E Chipset hardware and software to match the selected mode.

4.8.2.1 Ultra ATA/66 Motherboard Guidelines

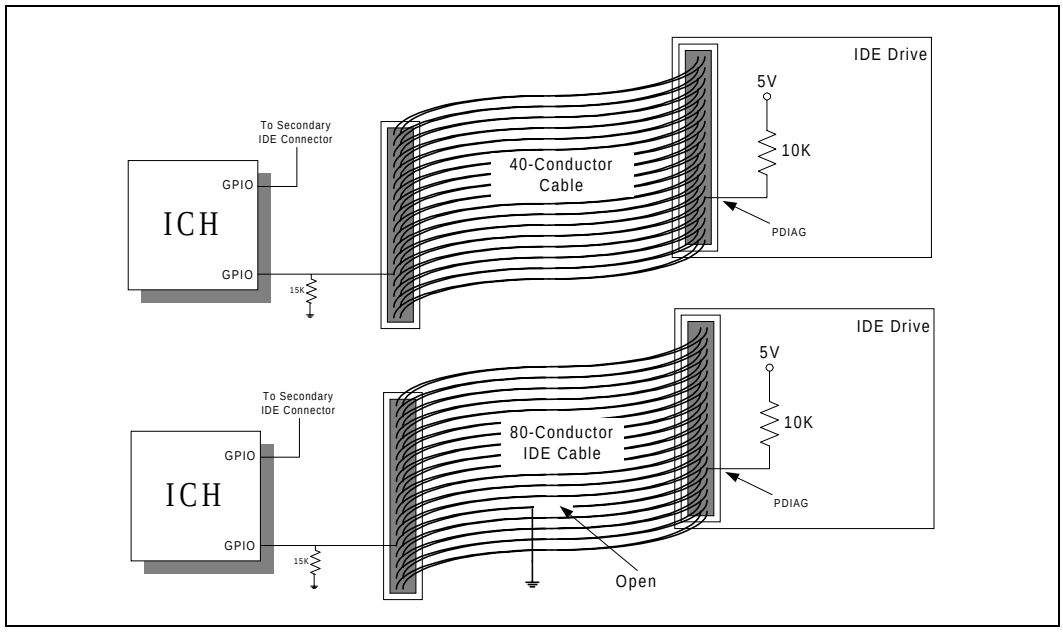
The Intel® 810E Chipset can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection—BIOS Detects Cable Type Using GPIOs

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 4-19. All Ultra ATA/66 devices have a 10K ohm pull-up resistor to 5 volts. Most of the GPIO pins on the ICH and all GPIs on FWH are not 5 volt tolerant. This requires a resistor divider so that 5 volts will not be driven to the ICH or FWH pins. The proper value of the series resistor is 15K ohm (as shown on Figure 4-19). This creates a 10K ohm/15K ohm resistor divider and will produce approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG#/CBLID#. If PDIAG#/CBLIB# is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG#/CBLID# is low then there is an 80-conductor cable in the system.

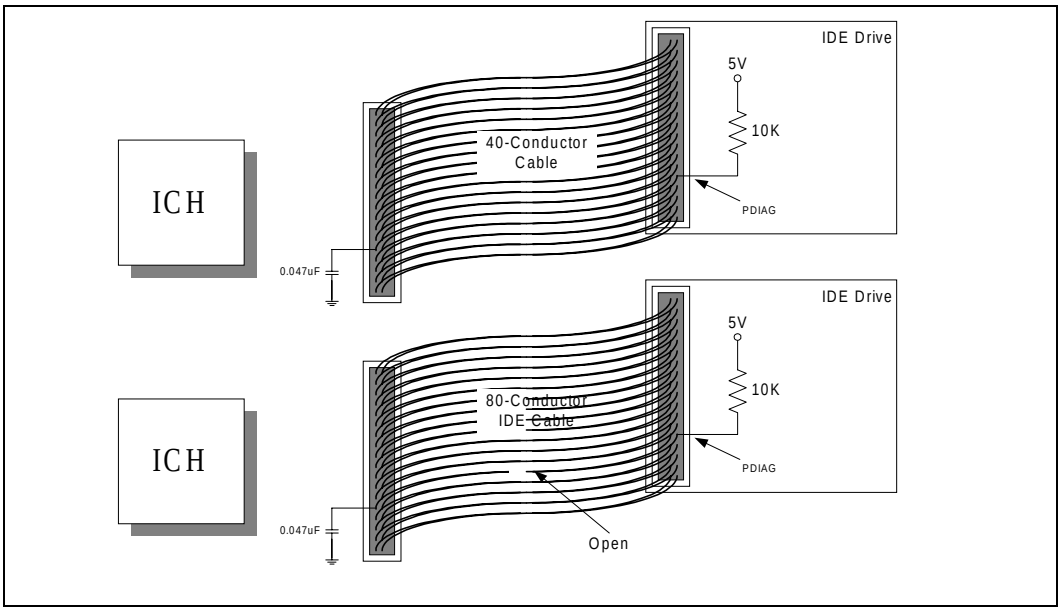
Figure 4-19. Host-Side IDE Cable Detection



Device-Side Detection—BIOS Queries IDE Drive for Cable Type

Device side detection requires only a 0.047 uF capacitor on the motherboard as shown in Figure 4-20. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10K ohm resistor). The drive will sample the PDIAG# signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through and therefore the capacitor has no effect. In a 40-conductor cable, PDIAG#/CBLID# is connected though to the drive. Therefore, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 4-20. Host-Side IDE Cable Detection

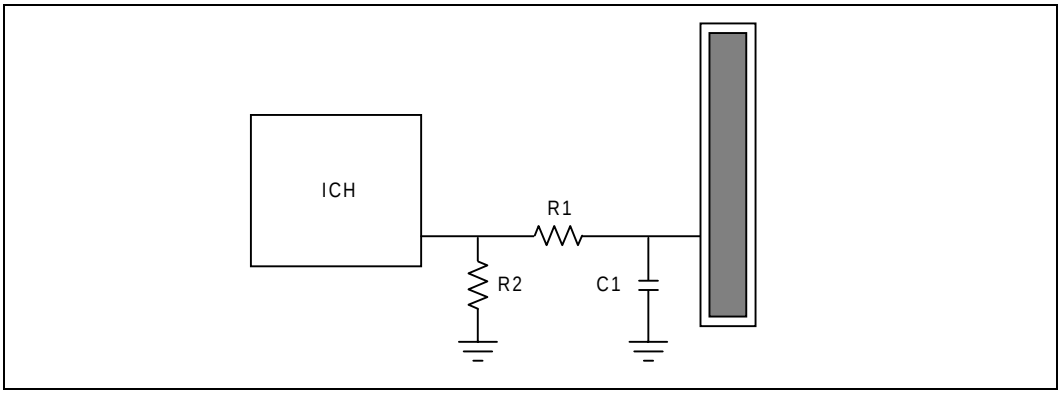


Layout for Both Host-Side and Drive-Side Cable Detection

It is possible to layout for both Host-Side and Drive-Side cable detection and decide the method to be used during assembly. Figure 4-21 shows the layout that allows for both host-side and drive-side detection.

- For Host-Side Detection
  - R1 is a 0 ohm resistor
  - R2 is a 15K ohm resistor
  - C1 is not stuffed
- For Drive-Side Detection
  - R1 is not stuffed
  - R2 is not stuffed
  - C1 is a 0.047 uF capacitor

Figure 4-21. Host-Side IDE Cable Detection



4.9 AC'97

The ICH implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH AC-link should be AC'97 2.1 compliant as well. Contact your preferred codec vendor for information on AC'97 2.1 compliant products. The AC'97 2.1 specification is on the Intel website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the following combinations of codecs:

Table 4-6. AC'97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in Table 4-6, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

4.9.1 Audio/Modem Riser Card (AMR)

Intel is developing a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options. The AMR specification is available on the Intel developer website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

4.9.2 AC'97 Routing

To ensure maximum performance from the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device specific recommendations.

Following are the basic recommendations:

- Special consideration must be given for the ground return paths for the analog signals. If isolated ground planes are used, pin B2 on the AMR connector should be used as an isolated ground pin and should be connected to an isolated ground plane to reduce noise in the analog circuits. The AMR designer and motherboard designer should jointly address any EMI issues when implementing isolated grounds.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in the other.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05" wide.
- Keep digital signal traces, especially the clock, as far way from analog input and voltage reference pins as possible.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (¼" to ½ " wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05" wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground (i.e., there should not be any signals crossing the split/gap between the ground planes). Doing so will cause a ground loop. This will greatly increase EMI emissions and degrade analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.
- Figure 4-22 and Figure 4-23 show the motherboard trace lengths for an ATX form factor with a codec on the motherboard and an AMR connector. Two routing methods are provided for the AC'97 interface: the tee topology and the daisy-chain topology. The AC'97 link signals can be routed using 5 mil traces with 5 mil space between the traces. NLX routing recommendations will be provided in a future revision of this document.

Figure 4-22. Tee Topology AC'97 Trace Length Requirements for ATX

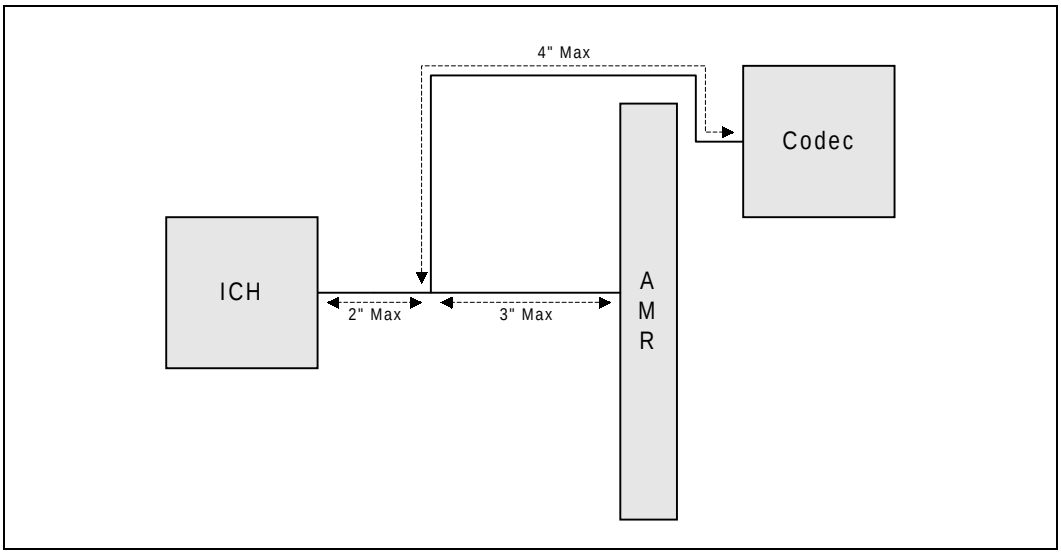
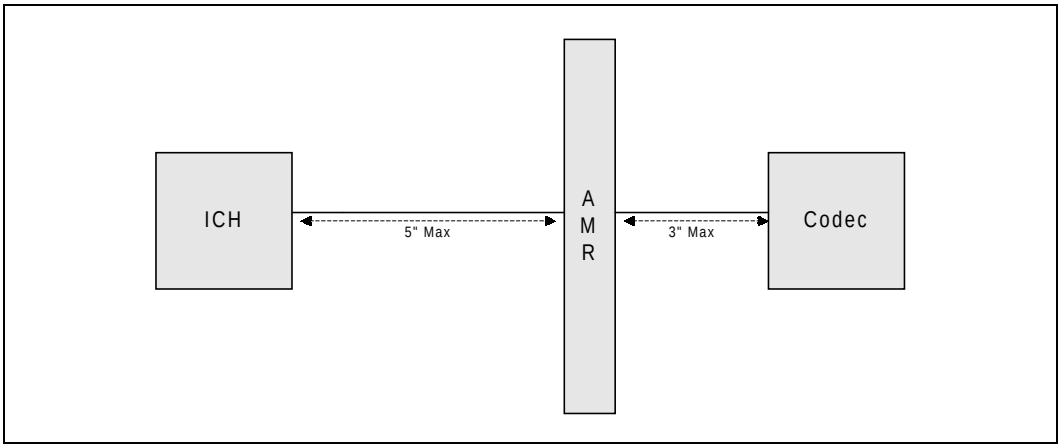


Figure 4-23. Daisy-Chain Topology AC'97 Trace Length Requirements for ATX



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH supports wake on ring from S1-S4 via the AC’97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If no codec is attached to the link, internal pulldowns will prevent the inputs from floating; therefore, external resistors are not required.

4.9.3 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components such as FET switches, buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing this will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH supports Wake On Ring from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns prevent the inputs from floating; therefore, external resistors are not required. The ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10K ohm) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If, however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.
  - In a lightly loaded system (e.g., single codec down), AC'97 signal integrity analysis should be evaluated to confirm that the signal quality on the link is acceptable by the codec used in the design. A series resistor at the driver and/or a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used are design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 5.

- AMR Slot Special Connections
  - AUDIO_MUTE#: No connect on the motherboard.
  - AUDIO_PWRDN: No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - MONO_PHONE: Connect top onboard audio codec if supported.
  - MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH, or MONO_OUT from onboard codec.
  - PRIMARY_DN#: See discussion above.
  - +5VDUAL/+5VSB: Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - S/P-DIF_IN: Connect to ground on the motherboard.
  - AC_SDATAIN[3:2]: No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

4.10 USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15K ohm pulldown resistors on both P+/P- data lines.
- 15 ohm series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible, and on the ICH side of the series resistors on the USB data lines (P0±, P1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15K ohm ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are for signal termination required by the USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0±, P1±- signals should be 45 ohms (to ground) for each USB signal P+ or P-. This may be achieved with 9 mil wide traces on the motherboard based on the stackup recommended in Figure 4-1. The impedance is 90 ohms between the differential signal pairs P+ and P- to match the 90 ohm USB twisted pair cable impedance. Note that the twisted pair characteristic impedance of 90 ohms is the series impedance of both wires, resulting in an individual wire presenting a 45 ohm impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals' (i.e., hand routing preferred). The P+/P- signal pair should be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. The P+/P- signal traces should also be the same length. This minimizes the effect of common mode current on EMI.

Figure 4-24 illustrates the recommended USB schematic.

Figure 4-24. USB Data Signals

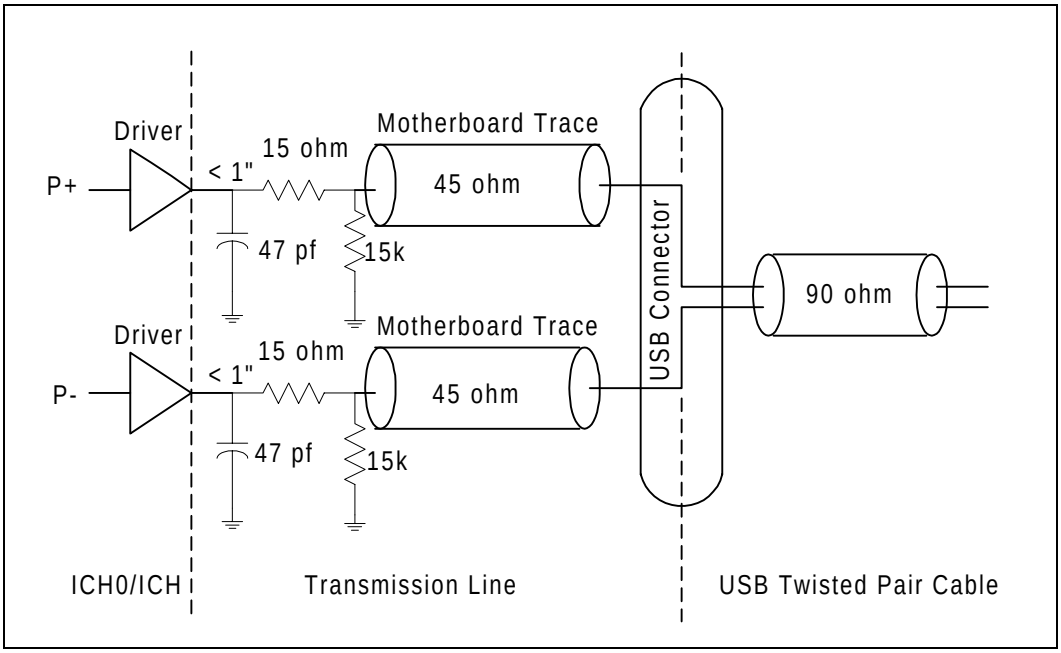


Table 4-7. Recommended USB Trace Characteristics

Impedance ‘Z0’ = 45.4 ohm
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Res @ 20° C = 53.9m ohm

4.11 IOAPIC (I/O Advanced Programmable Interrupt Controller)

Systems that do not use the ICH I/O APIC should follow these recommendations:

On the ICH:

- Tie PICCLK directly to ground
- Tie PICD0, PICD1 directly to ground

On the processor:

- PICCLK must be connected from the clock generator to the PICCLK pin on the processor
- Tie PICD0 to VCC_{CMOS} through a 150 ohm resistor
- Tie PICD1 to VCC_{CMOS} through a 150 ohm resistor

Note: If not using IOAPIC, turn off APIC clocks to ICH through I^2C.

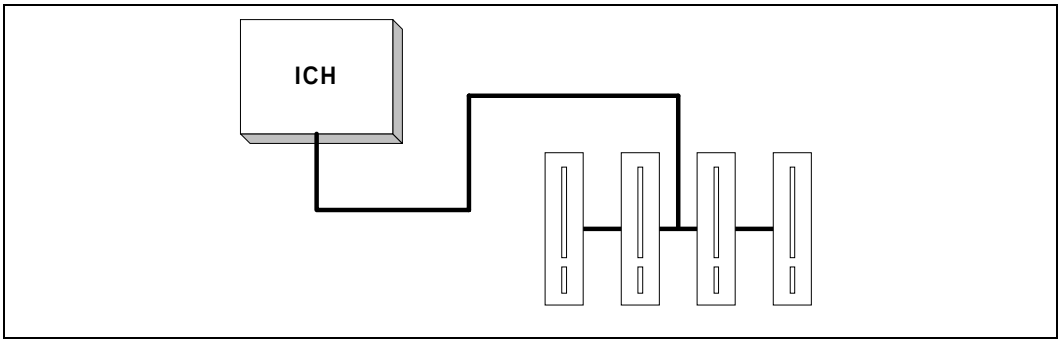
4.12 PCI

The ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH supports 6 PCI Bus masters (excluding ICH), by providing 6 REQ#/GNT# pairs. In addition, the ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

The ICH, based on simulations done by Intel, it is recommended that four is the maximum number of PCI slots that should be connected to the ICH. This limit is due to timing and loading considerations established during simulations. If a system designer wants to have 5 PCI slots connected to the ICH, then it is recommended that they do simulations to verify proper design.

Figure 4-25. PCI Bus Layout Example for 4 PCI Connectors



4.13 RTC

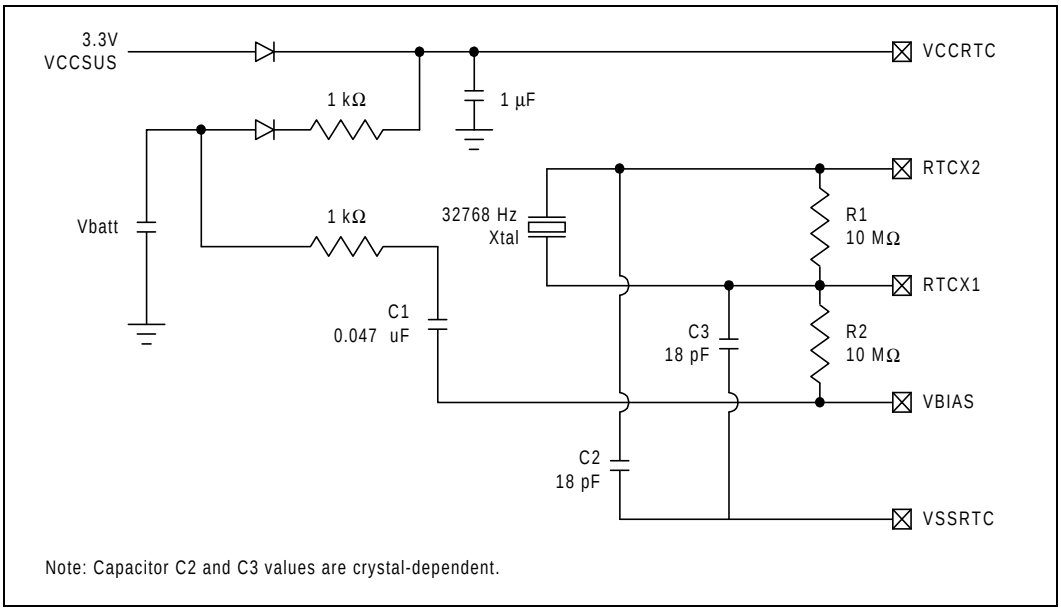
The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: a) keeping date and time, b) storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

4.13.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 4-26 represents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 4-26. External Circuitry for the ICH RTC



NOTES:
1. The exact capacitor value should be based on the crystal vendor's recommendations.
2. VccRTC: Power for RTC Well.
3. RTCX2: Crystal Input 2 – Connected to the 32.768 KHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 KHz crystal.
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground.

4.13.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 should be set to 0.047 uF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values (C2 and C3):

$$Cload = (C2*C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2; then, C2 can be trimmed to obtain the 32.768 KHz.

4.13.3 RTC Layout Considerations

- Keep the XTAL lead lengths as short as possible; around 1 inch is sufficient.
- Minimize the capacitance between RTCX1and RTCX2 in the routing.
- Put a ground plane under the XTAL components.
- Do not route any switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean; use a filter (e.g., an RC lowpass) or a ferrite inductor.
- Keep high speed switching signals (e.g., PCI signals) away from VCCRTC, RTCX1, RTCX2 and VBIAS.

4.13.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

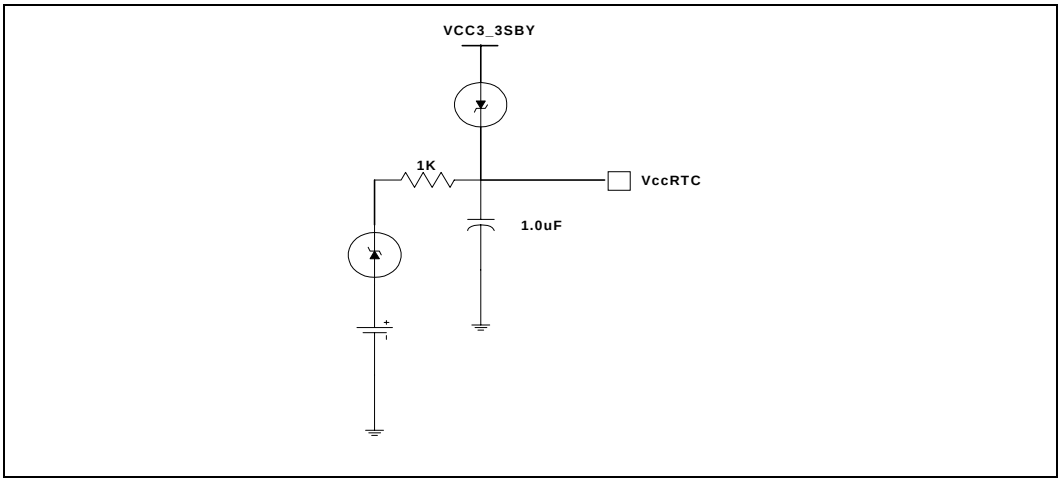
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mA per hour (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAhr / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse-biased when the system power is not available. Figure 4-27 is an example of a diode circuitry that can be used.

Figure 4-27. A Diode Circuit to Connect RTC External Battery

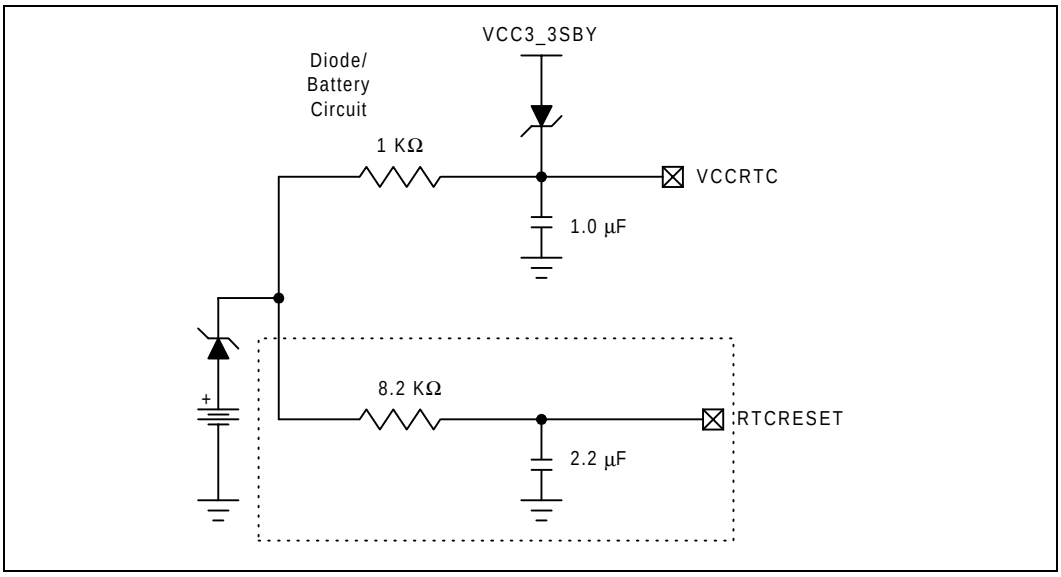


A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

4.13.5 RTC External RTCRESET Circuit

The ICH RTC requires some additional external circuitry. The RTCRESET (RTC Well Test) signal is used to reset the RTC Well. The external capacitor (2.2 uF) and the external resistor (8.2 KΩ) between RTCRESET and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRESET goes high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20 ms. When RTCRESET is asserted bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots, BIOS knows that the RTC battery has been removed.

Figure 4-28. RTCRESET External Circuit for the ICH RTC



This RTCRESET circuit is combined with the diode circuit (Figure 4-27) which allows the RTC well to be powered by the battery when the system power is not available. Figure 4-28 is an example of this circuitry that is used, in conjunction with the external diode circuit.

4.13.6 VBIAS DC Voltage and Noise Measurements

- Steady state VBIAS will be a DC voltage of about 0.38V ±.06V.
- VBIAS will be “kicked” when the battery is inserted to about 0.7–1.0V; it will come back to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum (200 mV or less).
- VBIAS is very sensitive and can not be directly probed; it can be probed through a 0.01 uF capacitor.
- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS it is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet.

4.14 Processor PLL Filter Recommendation

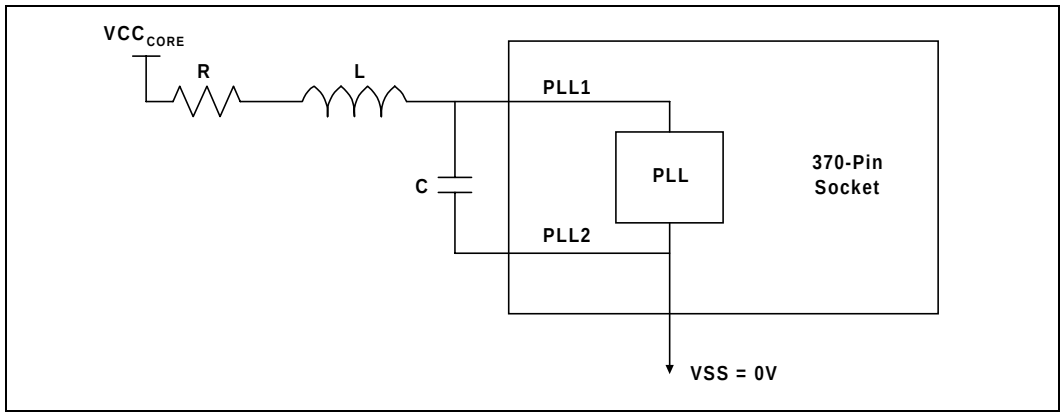
4.14.1 Processor PLL Filter Recommendation

All Intel® Celeron™ processors have internal PLL clock generators that are analog and require quiet power supplies to minimize jitter.

4.14.2 Topology

The general desired topology is shown in Figure 4-29. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

Figure 4-29. Filter Topology



4.14.3 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. In general, the low-pass description forms an adequate description for the filter.

The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

< 0.2 dB gain in pass band

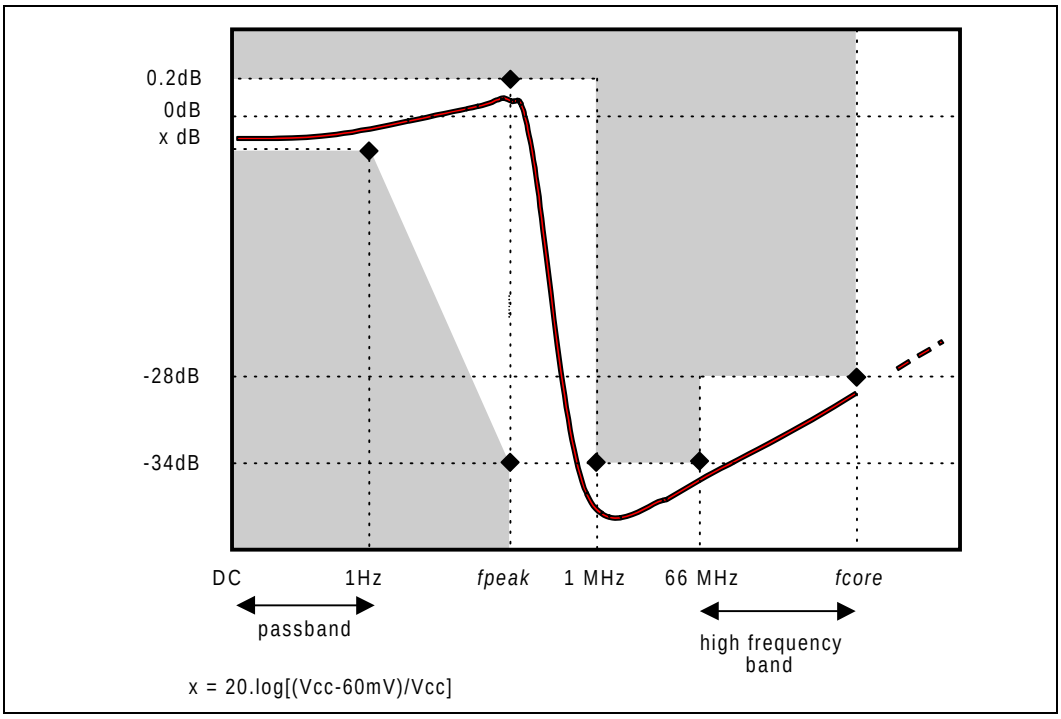
< 0.5 dB attenuation in pass band (see DC drop in next set of requirements)

> 34 dB attenuation from 1 MHz to 66 MHz

> 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 4-30.

Figure 4-30. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak,* if it exists, it should be less than 0.05 MHz.

Other requirements:

- Filter should support DC current > 30 mA.
- Shielded type inductor to minimize magnetic pickup.
- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2 ohm; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

4.14.4 Recommendation for Intel Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in the topology presented in Figure 4-29.

Table 4-8. Inductor

Part Number	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT	4.7 uH	10%	35 MHz	30 mA	0.56 ohm (1W max)
Murata LQG21N4R7K00T1	4.7 uH	10%	47 MHz	30 mA	0.7 ohm (±50%)
Murata LQG21C4R7N00	4.7 uH	30%	35 MHz	30 mA	0.3 ohm max

Table 4-9. Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 uF	20%	2.5 nH	0.225 ohm
AVX TPSD336M020S0200	33 uF	20%	TBD	0.2 ohm

Table 4-10. Resistor

Value	Tolerance	Power	Note
1 ohm	10%	1/16 W	Resistor may be implemented with trace resistance, in which discrete R is not needed

To satisfy damping requirements, total series resistance in the filter (from $V_{CC_{CORE}}$ to the top plate of the capacitor) must be at least 0.35 ohm. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has a minimum DCR of 0.25 ohm, then a routing resistance of at least 0.10 ohm is required. Be careful not to exceed the maximum resistance rule (2 ohm). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 ohm, which precludes using some inductors.

Other routing requirements:

- C should be close to PLL1 and PLL2 pins, < 0.1 ohm per route. These routes do not count towards the minimum damping R requirement.
- PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- L should be close to C; any routing resistance should be inserted between $V_{CC_{CORE}}$ and L.
- Any discrete R should be inserted between $V_{CC_{CORE}}$ and L.

Figure 4-31. Using Discrete R

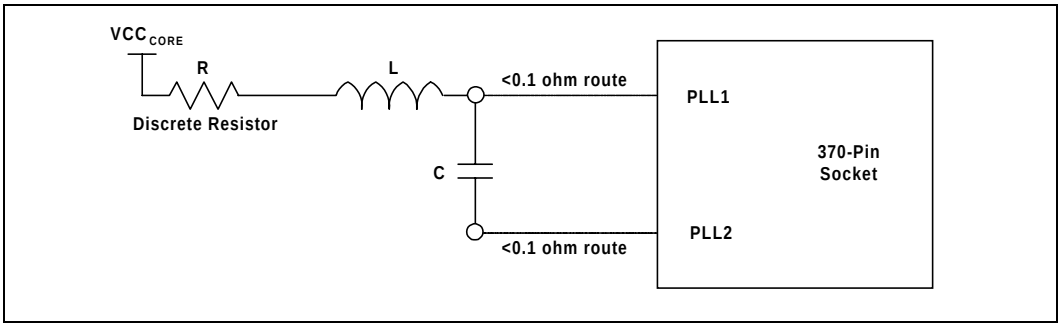
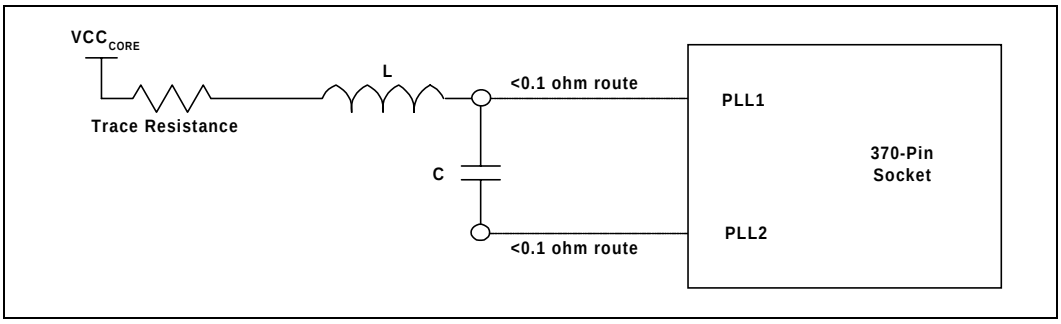


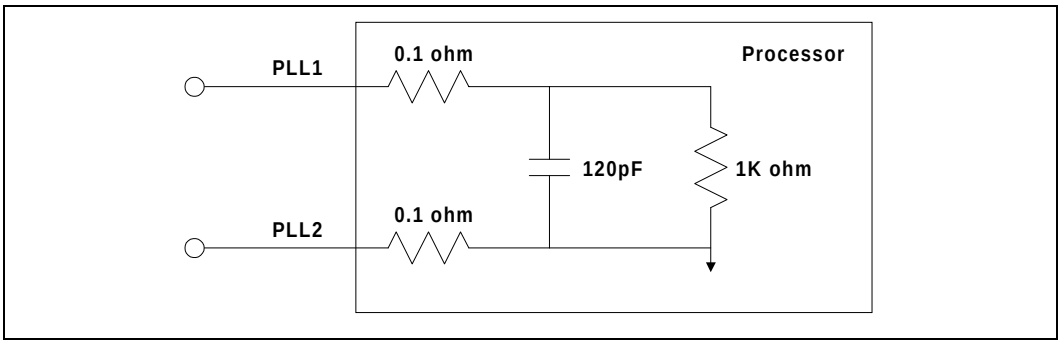
Figure 4-32. No Discrete R



4.14.5 Custom Solutions

As long as filter performance as specified in Figure 4-30 and other requirements outlined in Section 4.14.3, "Filter Specification" on page 4-29 are satisfied, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 4-33.

Figure 4-33. Core Reference Model



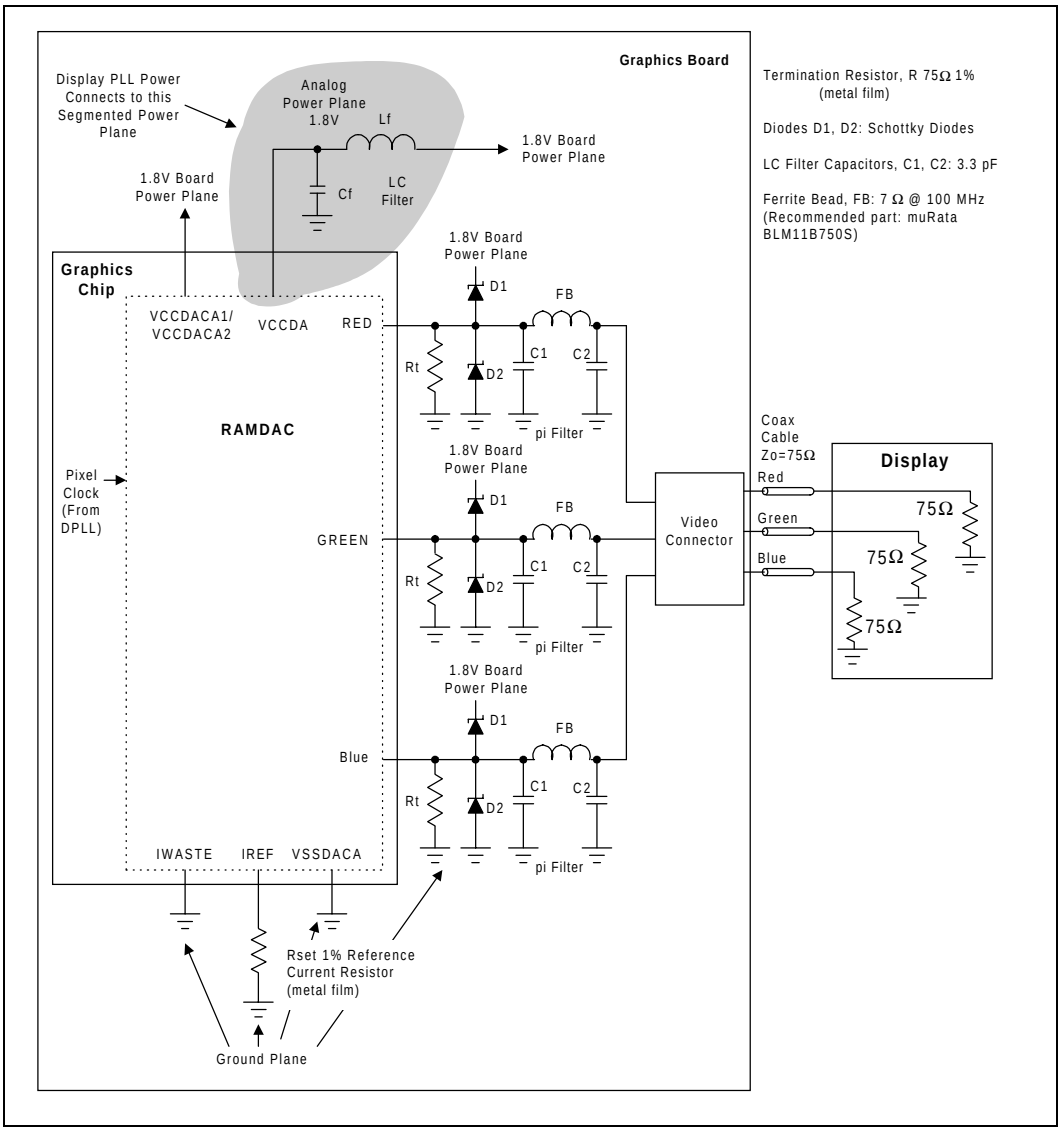
NOTES:
1. 0.1 ohm resistors represent package routing[1].
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1K ohm resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Please sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.

1. For other modules (interposer, DMM, etc), adjust routing resistor if desired, but use minimum numbers.

4.15 RAMDAC/Display Interface

Figure 4-34 shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly-terminated with a 75 ohm resistance; one 75 ohm resistance from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent dc resistance at the output of each DAC output is 37.5 ohm. The output current of each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter which is used to reduce high-frequency glitches and noise, and reduce EMI. To maximize the performance, the filter impedance, cable impedance and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a ferrite bead with a 75 ohm impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

Figure 4-34. Schematic of RAMDAC Video Interface



NOTE: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.8V power plane of the RAMDAC to the 1.8V board power plane. The LC filter is recommended to be designed for a cut-off frequency of 100 KHz.

4.15.1 Reference Resistor (Rset) Calculation

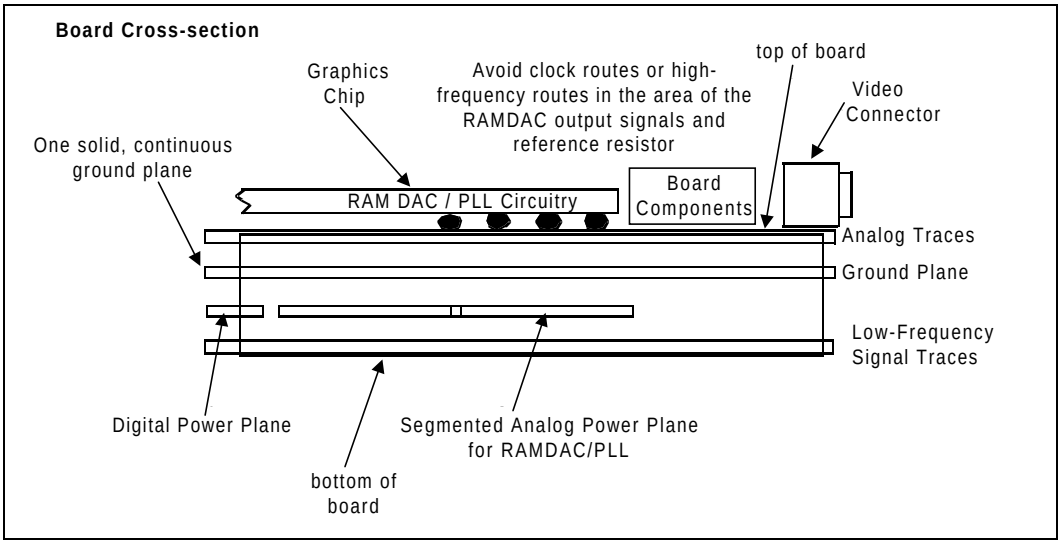
The full-swing video output is designed to be 0.7V according to the VESA video standard. With an equivalent dc resistance of 37.5 ohm (two 75 ohm in parallel - one 75 ohm termination on the board and one 75 ohm termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 ohm = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent 255I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this R_{set} resistor equal to a bandgap voltage divided-by-three (409 mV). The RAMDAC reference current generation circuitry is designed to generate a 32I reference current using the reference voltage and the R_{set} value. To generate a 32I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated from the following equation:

$$R_{set} = V_{REF}/32I = 0.409V/32*73.2\mu A = 174\ \Omega$$

4.15.2 RAMDAC Board Design Guidelines

Figure 4-35 shows a general cross-section of a typical four-layer board. The recommended RAMDAC routing for a four layer board is such that the red, green and blue video outputs be routed on the top (bottom) layer over (under) a solid ground plane to maximize noise rejection characteristics of the video outputs. It is essential to avoid toggling signals from being routed next to the video output signals to the VGA connector. A 20 mil spacing between any video route and any other routes is recommended.

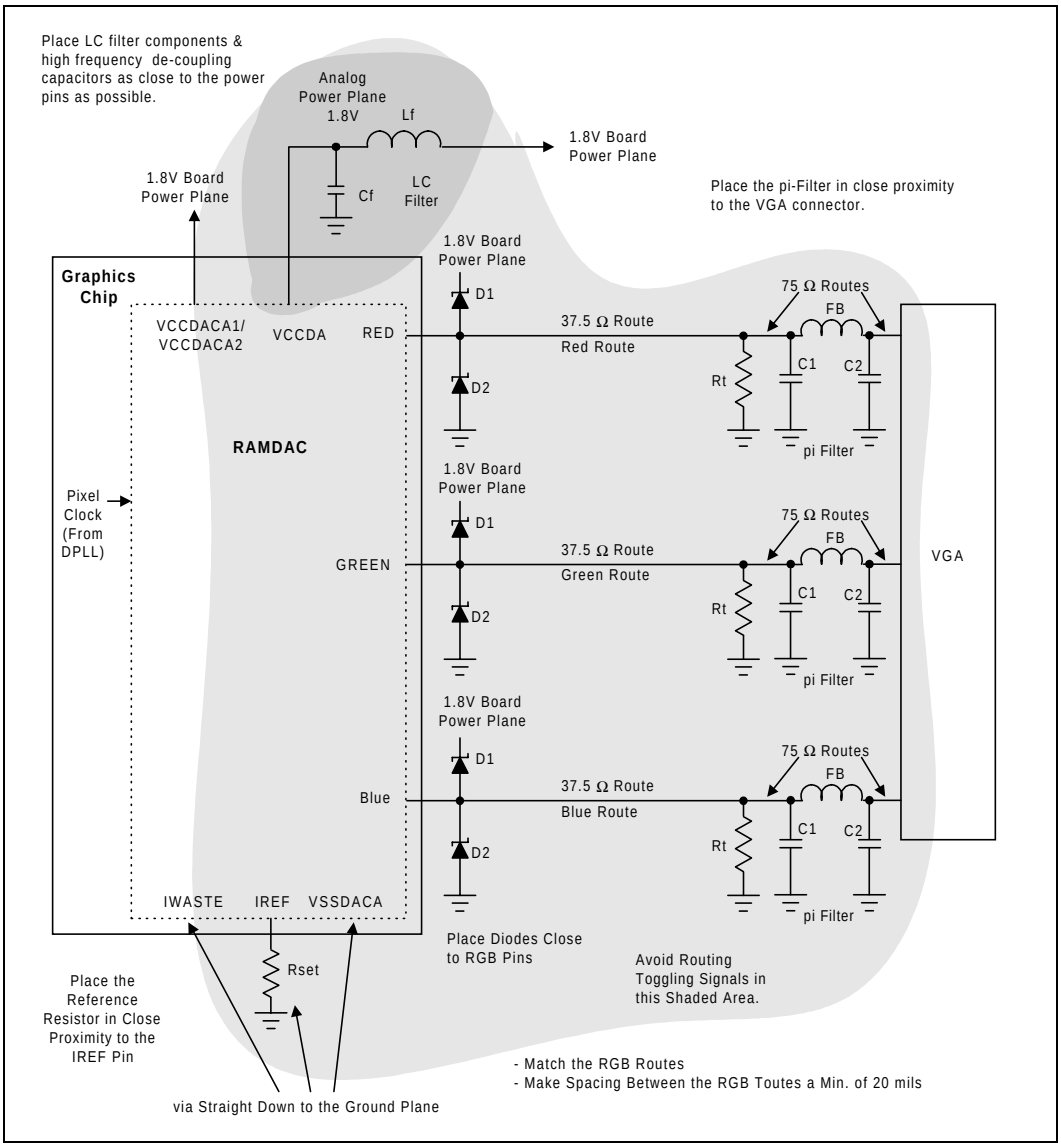
Figure 4-35. Cross-section View of a Four-Layer Board



Matching of the video routes (red, green, and blue) from the RAMDAC to the VGA connector is also essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs).

Figure 4-36 shows recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector as long as the impedance of the traces are designed as indicated in Figure 4-36. The pi-filters are recommended to be placed in close proximity to the VGA connector to maximize EMI filtering effectiveness. The LC filter components for the RAMDAC/PLL power plane, de-coupling capacitors, latch-up protection diodes, and the reference resistor are recommended to be placed in close proximity to the respective pins.

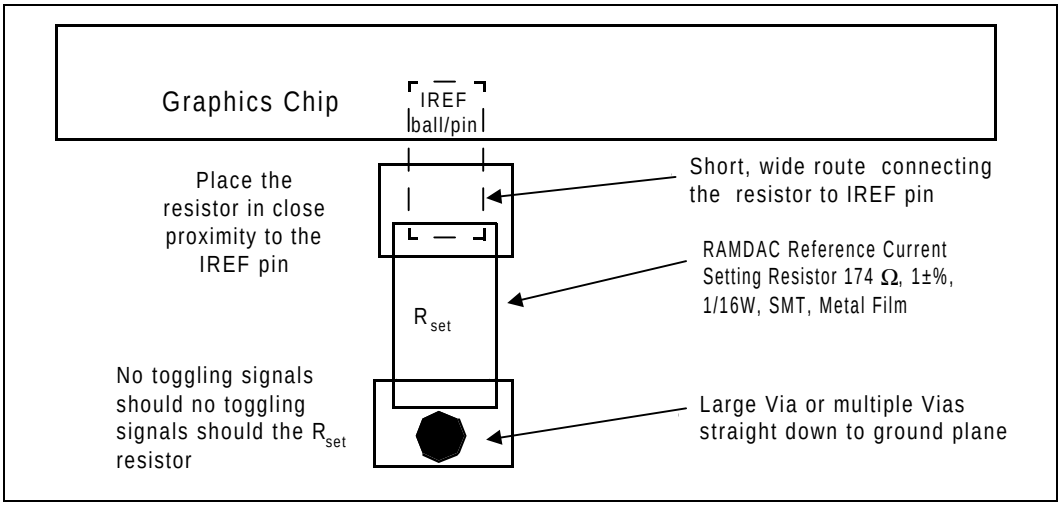
Figure 4-36. RAMDAC Component and Routing Guidelines



NOTE: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

Figure 4-37 shows the recommended reference resistor placement and connections.

Figure 4-37. Recommended RAMDAC Reference Resistor Placement and Connections



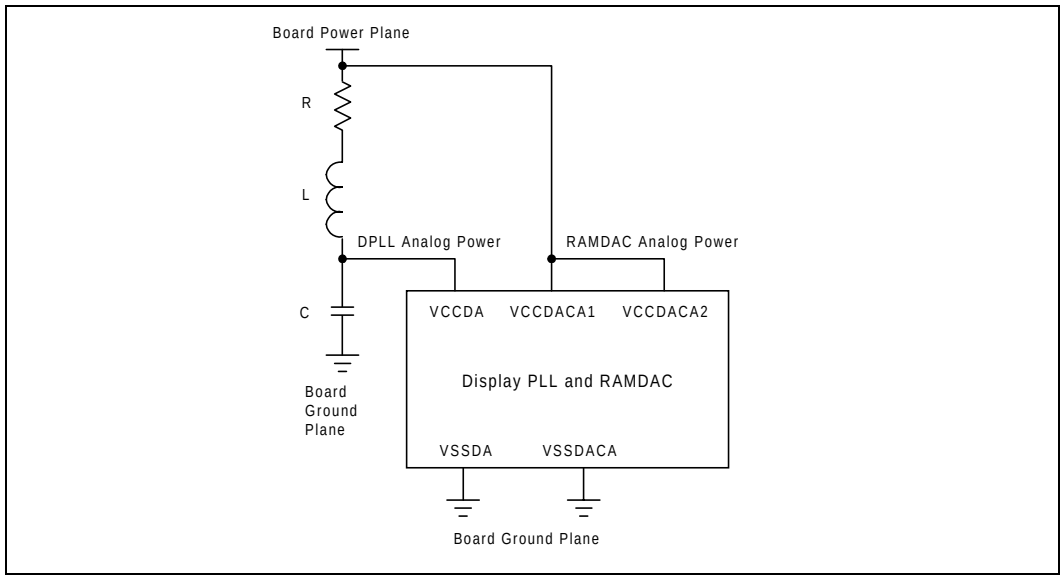
4.16 DPLL Filter Design Guidelines

The Intel® 810E Chipset contains sensitive phase-locked loop circuitry, the DPLL, that can cause excessive dot clock jitter. Excessive jitter on the dot clock may result in a “jittery” image. An LC filter network connected to the DPLL analog power supply is recommended to reduce dot clock jitter.

The DPLL bandwidth varies with the resolution of the display and can be as low as 100 KHz. In addition, the DPLL jitter transfer function can exhibit jitter peaking effects in the range from 100 KHz to a few megahertz. A low-pass LC filter is recommended for the display PLL analog power supply designed to attenuate power supply noise with frequency content from 100 KHz and above so that jitter amplification is minimized.

Figure 4-38 is a block diagram showing the recommended topology of the filter connection (parasitics not shown). The display PLL analog power rail (VCCDA) is connected to the board power plane through an LC filter. The RAMDAC analog power rail (VCCDACA1 and VCCDACA2) are connected directly to the 1.8V board power plane.

Figure 4-38. Recommended LC Filter Connection



The resistance from the inductor to the board 1.8V power plane represents the total resistance from the board power plane to the filter capacitor. This resistance, which can be a physical resistor, routing/via resistance, parasitic resistance of the inductor or combinations of these, acts as a damping resistance for the filter and effects the response of the filter.

The LC filter topology shown in Figure 4-38 is the preferred choice since the RAMDAC minimum voltage level requirement does not place constraints on the LC filter for the DPLL. The maximum current flowing into the DPLL analog power is approximately 30 mA, much less than that of the RAMDAC, and therefore, a filter inductor with a higher dc resistance can be tolerated. With the topology in Figure 4-38, the filter inductor dc current rating must be at least 30 mA and the maximum IR drop from the board power plane to the VCCDA ball should be 100 mV or less (corresponds to a series resistance equal to or less than 3.3 ohm. This larger dc resistance tolerance improves the damping and the filter response.

4.16.1 Filter Specification

The low-pass filter specification with the input being the board power plane and the output measured across the filter capacitor is defined as follows for the filter topology shown in Figure 4-38.

- pass band gain < 0.2 dB
- dc IR drop from board power plane to the DPLL VCCDA ball < 100 mV (and a maximum dc resistance < 3.3 ohm)
- filter should support a dc current > 30 mA
- minimum attenuation from 100 kHz to 10 MHz = 10 dB (desired attenuation > 20 dB)
- a magnetically shielded inductor is recommended

The resistance from the board power plane to the filter capacitor node should be designed to meet the filter specifications outlined above. This resistance acts as a damping resistance for the filter and affects the filter characteristics. This resistance includes the routing resistance from the board power plane connection to the filter inductor, the filter inductor parasitic resistance, the routing

from the filter inductor to the filter capacitor, and resistance of the associated vias. Part of this resistance can be a physical resistor. A physical resistor may not be needed depending on the resistance of the inductor and the routing/via resistance.

The filter capacitance should be chosen with as low of an ESR (equivalent series resistance) and ESL (equivalent series inductance) as possible to achieve the best filter performance. The parasitics of the filter capacitor can alter the characteristics of the filter significantly and even cause the filter to be ineffective at the frequencies of interest. The LC filter must be simulated with all the parasitics of the inductor, capacitor, and associated routing parasitics along with tolerances.

4.16.2 Recommended Routing/Component Placement

- The filter capacitance should be placed as close to the VCCDA ball as possible so that the routing resistance from the filter capacitor lead to the package VCCDA ball is < 0.1 ohm.
- The VSSDA ball should via straight down to the board ground plane.
- The filter inductor should be placed in close proximity to the filter capacitor and any routing resistance should be inserted between the board power plane connection and the filter inductor.
- If a discrete resistor is used for the LC filter, the resistor should be placed between the board power plane connection and the filter inductor.

4.16.3 Example LC Filter Components

Table 4-11 and Table 4-12 shows example LC components and resistance for the LC filter topology shown in Figure 4-38.

Table 4-11. DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 µF ±20%, 16VDC, ESR=0.225 ohm @ 100 kHz, ESL=2.5 nH
Inductor	muRATA	LQG11A68NJ00	68 nH ±5%, 300 mA, Max dc resistance = 0.8 ohm, size=0603
Resistance	—	—	< 3.3 ohm

The resistance of the filter is defined as the total resistance from the board power plane to the filter inductor. If a discrete resistor is used as part of this resistance, the tolerance and temperature coefficient should be accounted for so that the maximum dc resistance in this path from the board power plane connection to the DPLL VCCDA ball is less than 3.3 ohm to meet the IR drop requirement.

Table 4-12. Additional DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 µF ±20%, 16VDC, ESR=0.225 ohm @ 100 kHz, ESL=2.5 nH
Inductor	muRATA	LQG21NR10K10	100 nH ±10%, 250 mA, Max dc resistance = 0.26 ohm, size=0805, magnetically shielded

As an example, Figure 4-39 is a Bode plot showing the frequency response using the capacitor and inductor values shown in Table 4-12. The capacitor and inductor values were held constant while the resistance was swept for four different combinations of resistance (the resistance of the discrete/trace resistor and the resistance of the inductor), each resulting in a different series resistance. In addition, different values for the resistance of the inductor were assumed based on its max and typical DC resistance. This is summarized in Table 4-13. This yielded the four different frequency response curves shown in Figure 4-39.

Figure 4-39. Frequency Response (see Table 4-13)

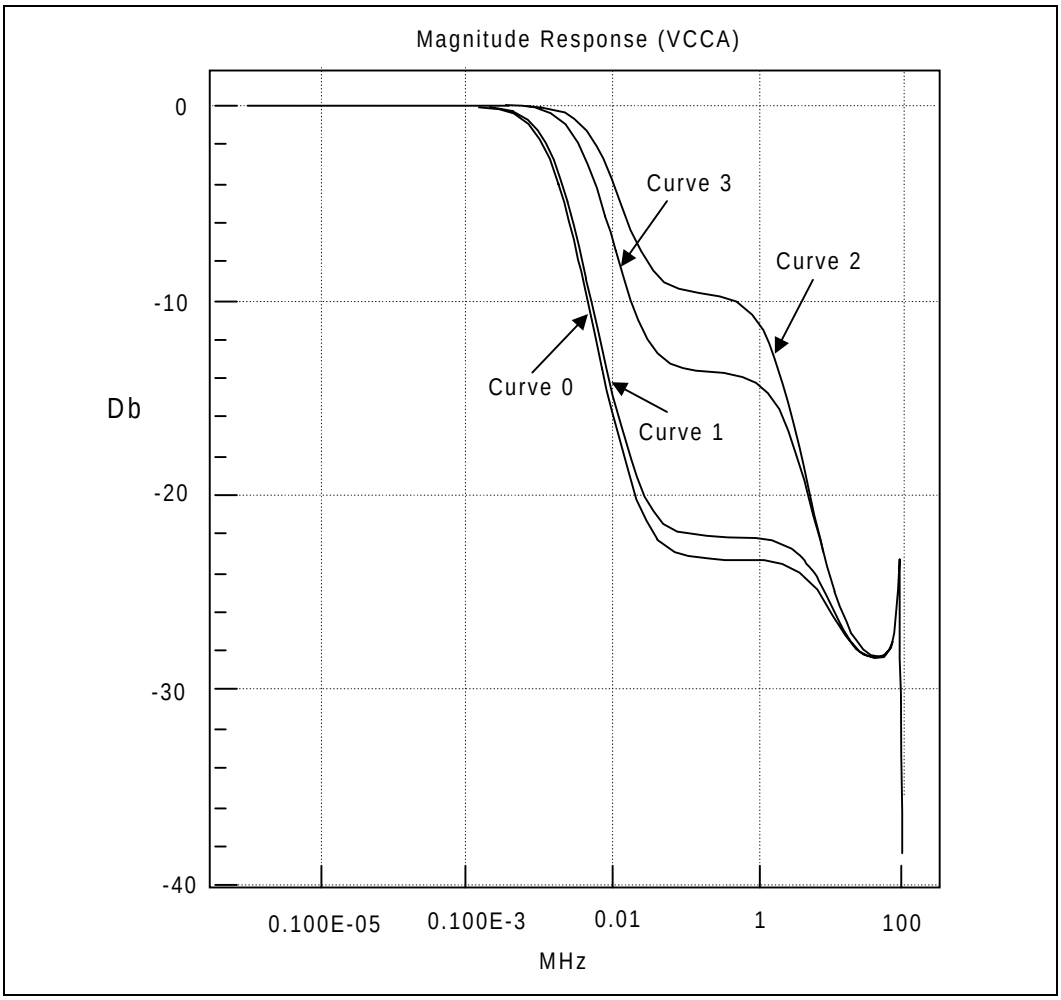


Table 4-13. Resistance Values for Frequency Response Curves (see Figure 4-39)

Curve	$R_{TRACE} + R_{DISCRETE}$	R_{IND}
0	2.2 ohm	0.8 ohm
1	2.2 ohm	0.4 ohm
2	0 ohm	0.4 ohm
3	0 ohm	0.8 ohm

As series resistance ($R_{TRACE} + R_{DISCRETE} + R_{IND}$) increases, the filter response (i.e., attenuation in PLL bandwidth) improves. There is a limit of 3.3 ohm total series resistance of the filter to limit DC voltage drop.



5

Advanced System Bus

Advanced System Bus Design 5

This chapter discusses more detail about the methodology used to develop the guidelines. Section 5.1, “AGTL+ Design Guidelines” on page 5-1 discusses specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design high performance desktop systems. Section 5.2, “Theory” on page 5-12 introduces the theories that are applicable to this layout guideline. Section 5.3, “More Details and Insight” on page 5-16 contains more details and insights. The items in Section 5.3 expand on some of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

5.1 AGTL+ Design Guidelines

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 82810E GMCH load. Systems using custom chipsets will require timing analysis and analog simulations specific to those components.

The guideline recommended in this section is based on experience developed at Intel while developing many different Intel Pentium® Pro processor family and Intel Pentium III processor-based systems. Begin with an initial timing analysis and topology definition. Perform pre-layout analog simulations for a detailed picture of a working “solution space” for the design. These pre-layout simulations help define routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial Timing Analysis
- Determine General Topology, Layout, and Routing
- Pre-Layout Simulation
  - — Sensitivity sweep
  - — Monte Carlo Analysis
- Place and Route Board
  - — Estimate Component to Component Spacing for AGTL+ Signals
  - — Layout and Route Board
- Post-Layout Simulation
  - — Interconnect Extraction
  - — Inter-Symbol Interference (ISI), Cross-talk, and Monte Carlo Analysis
- Validation
  - — Measurements
  - — Determining Flight Time

5.1.1 Initial Timing Analysis

Perform an initial timing analysis of the system using Equation 5-1 and Equation 5-2 shown below. These equations are the basis for timing analysis. To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, M_{ADJ}, to account for multi-bit switching effects such as SSO pushout or pull-in that are often hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

Equation 5-1. Setup Time

$$T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{FLT\_MAX} + M_{ADJ} \leq \text{Clock Period}$$

Equation 5-2. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} - M_{ADJ} \geq T_{HOLD} + CLK_{SKEW}$$

Symbols used in Equation 5-1 and Equation 5-2:

- T_{CO_MAX} is the maximum clock to output specification[1].
- T_{SU_MIN} is the minimum required time specified to setup before the clock[1].
- CLK_{JITTER} is the maximum clock edge-to-edge variation.
- CLK_{SKEW} is the maximum variation between components receiving the same clock edge.
- T_{FLT_MAX} is the maximum flight time as defined in Section 1.1.1, “Terminology and Definitions” on page 1-2.
- T_{FLT_MIN} is the minimum flight time as defined in Section 1.1.1, “Terminology and Definitions” on page 1-2.
- M_{ADJ} is the multi-bit adjustment factor to account for SSO pushout or pull-in.
- T_{CO_MIN} is the minimum clock to output specification[1].
- T_{HOLD} is the minimum specified input hold time.

Note: The Clock to Output (T_{CO}) and Setup to Clock (T_{SU}) timings are both measured from the signals last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the respective Processor’s datasheet and the *Pentium® III Processor Developer’s Manual* for more details.

Solving these equations for T_{FLT} results in the following equations:

Equation 5-3. Maximum Flight Time

$$T_{FLT\_MAX} \leq \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

Equation 5-4. Minimum Flight Time

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

There are multiple cases to consider. Note that while the same trace connects two components, component A and component B, the minimum and maximum flight time requirements for component A driving component B as well as component B driving component A must be met. The cases to be considered are:

- Processor driving processor
- Processor driving chipset
- Chipset driving processor

A designer using components other than those listed above must evaluate additional combinations of driver and receiver.

Table 5-1. AGTL+ Parameters for Example Calculations[1,2]

IC Parameters	Intel® Pentium® III processor core at 133 MHz Bus	Intel 82810E GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	2.7	3.6	4
Clock to Output minimum (T_{CO_MIN})	-0.1	0.5	4
Setup time (T_{SU_MIN})	1.2	2.27	3,4
Hold time (T_{HOLD})	0.8	0.28	4

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 1.9 ns assumes the **82**810E GMCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Pentium III substrate nominal impedance is set to 65 Ω ±15%. Future Pentium III processor substrate may be set at 60 Ω ±15%

Table 5-1 lists the AGTL+ component timings of the processors and 82810E GMCH defined at the pins. These timings are for reference only.

Table 5-2 gives an example AGTL+ initial maximum flight time and Table 5-3 is an example minimum flight time calculation for a 133 MHz, 2-way Pentium III processor/Intel 810E chipset system bus. Note that assumed values for clock skew and clock jitter were used. Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Intel highly recommends adding margin as shown in the "M_{ADJ}" column to offset the degradation caused by SSO push-out and other multi-bit switching effects. The "Recommended T_{FLT_MAX}" column contains the recommended maximum flight time after incorporating the M_{ADJ} value. If edge rate, ringback, and monotonicity requirements are not met, flight time correction must first be performed as documented in the *Pentium® II Processor Developer's Manual* with the additional requirements noted in Section 5.4, "Definitions of Flight Time Measurements/Corrections and Signal Quality" on page 5-21. The commonly used "textbook" equations used to calculate the expected signal propagation rate of a board are included in Section 5.1, "AGTL+ Design Guidelines" on page 5-1.

Simulation and control of baseboard design parameters can ensure that signal quality and maximum and minimum flight times are met. Baseboard propagation speed is highly dependent on transmission line geometry configuration (stripline vs. microstrip), dielectric constant, and loading. This layout guideline includes high-speed baseboard design practices that may improve the amount

of timing and signal quality margin. The magnitude of M_{ADJ} is highly dependent on baseboard design implementation (stackup, decoupling, layout, routing, reference planes, etc.) and needs to be characterized and budgeted appropriately for each design.

Table 5-2 and Table 5-3 are derived assuming:

- CLK_{SKEW} = 0.2 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.)
- CLK_{JITTER} = 0.250 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the appropriate Intel 810E chipset documentation and *CK98 Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Refer to Chapter 6, "Clocking" for host clock routing details.

Table 5-2. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	Processor	7.50	2.7	1.20	0.20	0.250	0.40	2.75
Processor	82810E GMCH	7.50	2.7	2.27	0.20	0.250	0.40	1.68
82810E GMCH	Processor	7.50	3.63	1.20	0.20	0.25	0.40	1.82

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   - The effective board propagation constant (S_{EFF}), which is a function of:
     - Dielectric constant (ε_r) of the PCB material.
     - The type of trace connecting the components (stripline or microstrip).
     - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.

Table 5-3. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	Processor	0.8	0.2	-0.1	1.2
Processor	82810E GMCH	0.28	0.2	-0.1	.58
82810E GMCH	Processor	0.8	0.2	0.5	.5

NOTE: All times in nanoseconds.

5.1.2 Determine General Topology, Layout, and Routing Desired

After calculating the timing budget, determine the approximate location of the processor and the chipset on the base board.

5.1.3 Pre-Layout Simulation

5.1.3.1 Methodology

Analog simulations are recommended for high speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working “solution space” that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

5.1.3.2 Sensitivity Analysis

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

5.1.3.3 Monte Carlo Analysis

Perform a Monte Carlo analysis to refine the passing solution space region. A Monte Carlo analysis involves randomly varying parameters (independent of one another) over their tolerance range. This analysis intends to ensure that no regions of failing flight time and signal quality exists between the extreme corner cases run in pre-layout simulations. For the example topology, vary the following parameters during Monte Carlo simulations:

- Lengths L1 through L3
- Termination resistance R_{TT} on the processor cartridge #1
- Termination resistance R_{TT} on the processor cartridge #2
- Z_0 of traces on processor cartridge #1
- Z_0 of traces on processor cartridge #2
- S_0 of traces on processor cartridge #1
- S_0 of traces on processor cartridge #2
- Z_0 of traces on baseboard
- S_0 of traces on baseboard
- Fast and slow corner processor I/O buffer models for cartridge #1
- Fast and slow corner processor I/O buffer models for cartridge #2
- Fast and slow package models for processor cartridge #1
- Fast and slow package models for processor cartridge #2
- Fast and slow corner 82810E GMCH I/O buffer models
- Fast and slow 82810E GMCH package models

5.1.3.4 Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 ohm*mil^2/inch, not the 0.662 ohm*mil^2/inch value for annealed copper that is published in reference material. Using the 1 ohm*mil^2/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst-case noise margin. Therefore, Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that **both fast and slow corner conditions** must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher V_{OL}. So, Intel **highly recommends** checking for minimum and maximum flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 810E chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z0 and S0. Intel therefore recommends that PCB parameters are controlled as tightly as possible, with a sampling of the allowable Z0 and S0 simulated. The Intel® Pentium® III processor nominal effective line impedance is 65 Ω ±15%. Future Intel® Pentium® III processor effective line impedance (Z_{EFF}) may be 60 Ω ±15%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω ±15% for the recommended layout guidelines to be effective. Intel also recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for cross-talk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This lead to the development of full package models for the component packages.

5.1.4 Place and Route Board

5.1.4.1 Estimate Component To Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 5-2 and Table 5-3 assume values for CLK_{SKEW} and CLK_{JITTER} - parameters that are controlled by the system designer. To reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

5.1.4.2 Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible (but do not forget minimum component-to-component distances to meet hold times).
- Plan to minimize cross-talk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations - spacing may be decreased based upon the amount of coupled length):
  - Use a spacing to line width to dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.
  - Minimize the dielectric process variation used in the PCB fabrication.
  - Eliminate parallel traces between layers not separated by a power or ground plane.

Figure 5-3 contains the trace width:space ratios assumed for this topology. The cross-talk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intra-group AGTL+ cross-talk involves interference between AGTL+ signals within the same group (See Section 5.3, “More Details and Insight” on page 5-16 for a description of the different AGTL+ group types). Intergroup AGTL+ cross-talk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is when CMOS and AGTL+ signals interfere with each other.

Table 5-4. Trace Width Space Guidelines

Cross-talk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. A reduction of noise may be obtained by a minimum spacing between the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Therefore, adjusting the inter-agent spacing may be one way to change the network’s noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two or more agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. The ring-back from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This document addresses AGTL+ layout for both 1 and 2-way 133 MHz/100 MHz processor/ Intel® 810E chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location; therefore, constraining the board routing. These issues are not directly addressed in this document. **Section 1.1.2, “References” on page 1-7 c**ontains a listing of several documents that address some of these issues.

5.1.4.3 Host Clock Routing

Host clock nets should be routed as point-to-point connections through a series resistor placed as close to the output pins of the clock driver as possible. The value of the series resistor is dependent on the clock driver characteristic impedance. However, a value of 33 Ω is a good starting point. Table 5-5 provides the trace length recommendations for this topology. “H” indicates the length of the host clock trace starting from the clock driver output pin and ending at the SC242 connector BCLK pin. Note that the clock route from the clock driver to the Intel 82810E GMCH will require an additional trace length of approximately 4.6” to compensate for the additional propagation delay along the processor host clock path (SC242 connector plus processor cartridge trace). This value of 4.6” assumes a propagation speed of 180 ps/in.

Table 5-5. Host Clock Routing

Clock Net	Trace length
Clock driver to SC242 connector	H
Clock driver to Intel 82810E GMCH	H + (clock delay from the processor edge to core) + connector delay

5.1.4.4 APIC Data Bus Routing

Intel recommends using the in-line topology shown in Figure 5-1 and Figure 5-2 for the APIC Data signals, PICD[1:0]. For dual-processor systems, the network should be dual-end terminated with 330 Ω resistors. The combined routing lengths of L1 plus L2 should be between 0.0” and 12.0”.

Figure 5-1. PICD[1,0] Uni-Processor Topology

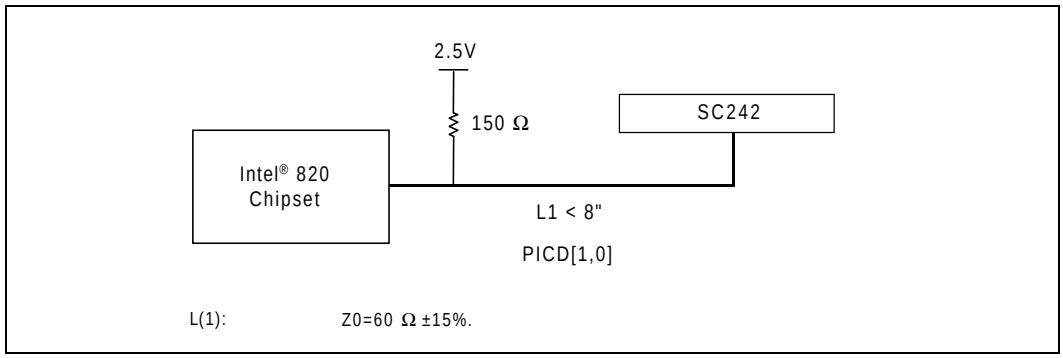
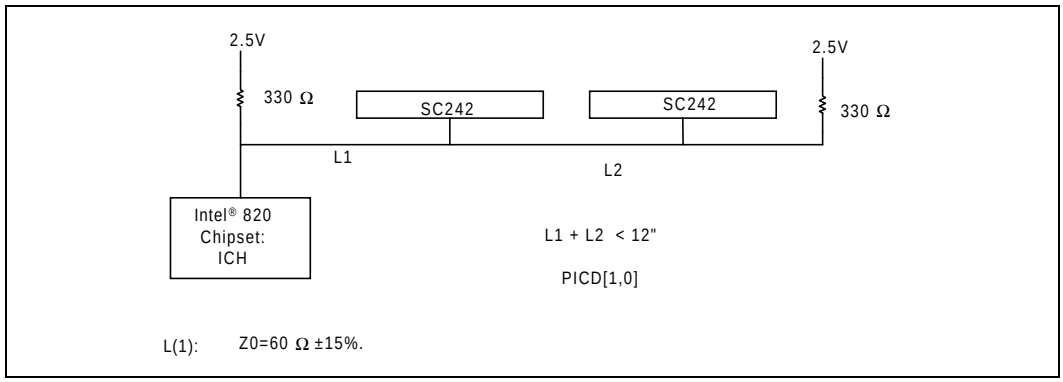


Figure 5-2. PICD[1,0] Dual-Processor Topology



5.1.5 Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

5.1.5.1 Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only 3 cycles so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

5.1.5.2 Cross-Talk Analysis

AGTL+ cross-talk simulations can consider the processor core package, Intel 82810E GMCH package, and SC242 connectors as non-coupled. Treat the traces on the processor cartridge and baseboard as fully coupled for maximum cross-talk conditions. Simulate the traces as lossless for worst case cross-talk and lossy where more accuracy is needed. Evaluate both odd and even mode cross-talk conditions.

AGTL+ Cross-talk simulation involves the following cases:

- Intra-group AGTL+ cross-talk
- Inter-group AGTL+ cross-talk
- Non-AGTL+ to AGTL+ cross-talk

5.1.5.3 Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

5.1.6 Validation

Build systems and validate the design and simulation assumptions.

5.1.6.1 Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

5.1.6.2 Flight Time Simulation

As defined in Section 1.1.1, “Terminology and Definitions” on page 1-2, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver, and the output pin of the driver crossing V_{REF} were it driving a test load. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 Ω and is equal to the test load. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively “sees” a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the cartridge.

Figure 5-3. Test Load vs. Actual System Load

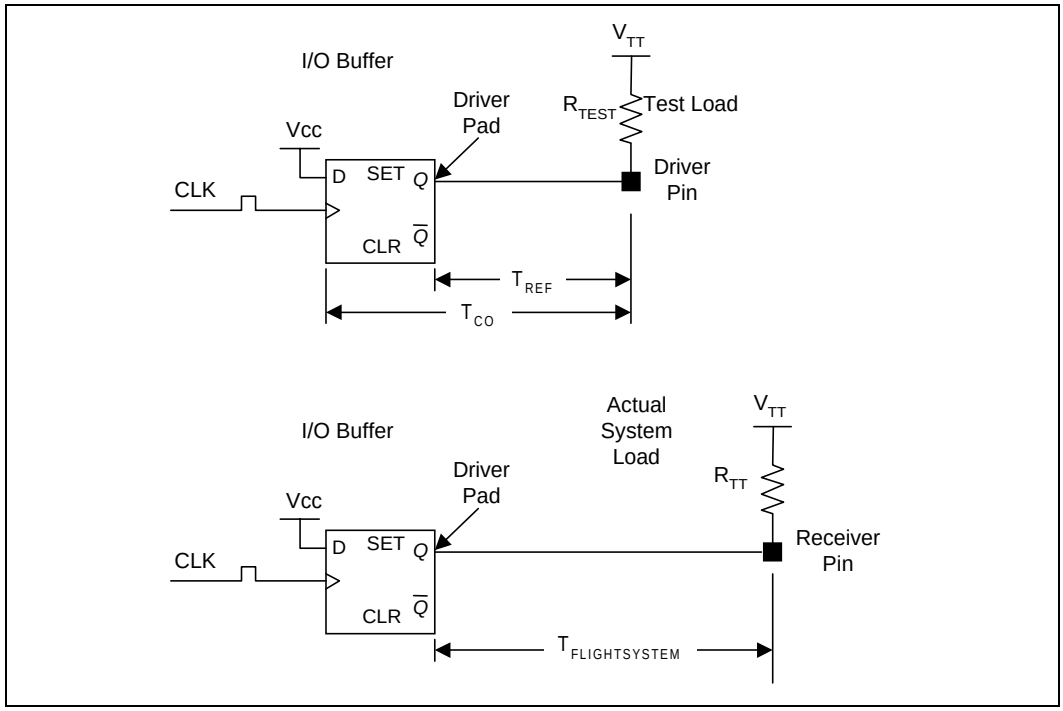


Figure 5-3 above shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver’s input pin sees a valid data input. Since both timing numbers (T_{CO} and $T_{FLIGHT-SYSTEM}$) include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid

double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following *valid delay* equation is satisfied:

Equation 5-5. Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT\text{-}SYS} - T_{REF} = T_{CO\text{-}MEASURED} + T_{FLIGHT\text{-}MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

5.1.6.3 Flight Time Hardware Validation

When a measurement is made on the actual system, T_{CO} and flight time do not need T_{REF} correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface and the same is true for the T_{CO}. Therefore the addition of the measured T_{CO} and the measured flight time must be equal to the valid delay calculated above.

5.2 Theory

5.2.1 AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage (V_{TT}).
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT}).
- processor termination resistance (R_{TT}).
- Input low voltage (V_{IL}).
- Input high voltage (V_{IH}).
- NMOS on resistance (RON_N).
- PMOS on resistance (RON_P).
- Edge rate specifications.
- Ringback specifications.
- Overshoot/Undershoot specifications.
- Settling Limit.

5.2.2 Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.
  - Clock to output [T_{CO}]. (Note that the system load is likely to be different from the "specification" load therefore the T_{CO} observed in the system might not be the same as the T_{CO} from the specification.)
  - The minimum required setup time to clock [T_{SU_MIN}] for each receiving agent.
- The range of flight time between each component. This includes:
  - The velocity of propagation for the loaded printed circuit board [S_{EFF}].
  - The board loading impact on the effective T_{CO} in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to cross-talk, noise, and other effects.

5.2.3 Cross-Talk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of cross-talk than they may have been in past designs.

Cross-talk is caused through capacitive and inductive coupling between networks. Cross-talk appears as both backward cross-talk and as forward cross-talk. Backward cross-talk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. Figure 5-4 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes cross-talk on the victim network.

Figure 5-4. Aggressor and Victim Networks

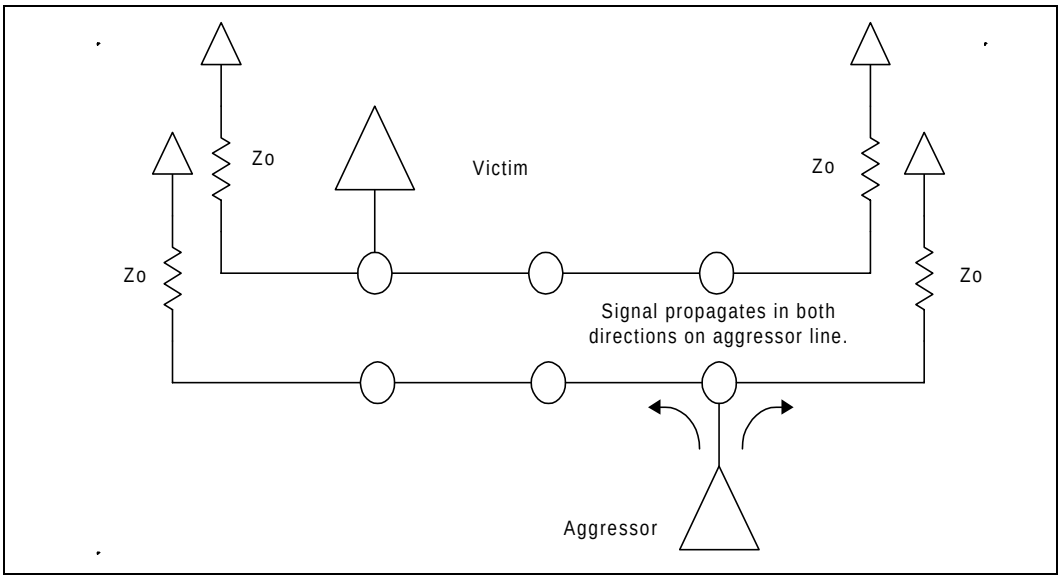
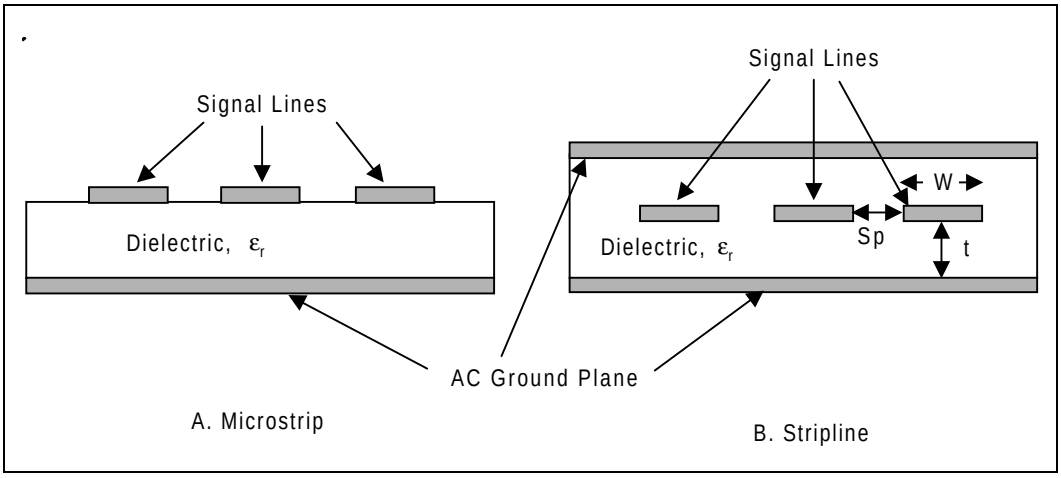


Figure 5-5. Transmission Line Geometry: (A) Microstrip (B) Stripline



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because cross-talk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum cross-talk occurs when all the aggressors are switching in the same direction at the same time.

There is cross-talk internal to the IC packages, which can also affect the signal quality.

Backward cross-talk is present in both stripline and microstrip geometry's (see Figure 5-5). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires **stripping** a layer away to see the signal lines. The backward coupled amplitude is proportional to the backward cross-talk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward cross-talk reaches a maximum (and remains constant) when the

propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

$$LengthforMaxBackwardCrosstalk = \frac{\frac{1}{2} \times FallTime}{BoardDelayPerUnitLength}$$

An example calculation follows when the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot):

Fall time = 1.5 V÷3 V/ns = 0.5 ns

Length for Max Backward Cross-talk

= ½ * 0.5 ns * 1000 ps/ns ÷175 ps/in

= 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward cross-talk from segments on two sides of a driver. The pulses from the backward cross-talk travel toward each other and meet and **add** at certain moments and positions on the bus. This can cause the voltage (noise) from cross-talk to double.

5.2.3.1 Potential Termination Cross-Talk Problems

The use of commonly used "pull-up" resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

5.3 More Details and Insight

5.3.1 Textbook Timing Equations

The “textbook” equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters. These equations are:

Equation 5-6. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega)$$

Equation 5-7. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$

Equation 5-8. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \quad \text{(ns/ft)}$$

Equation 5-9. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \quad \text{(ns/ft)}$$

Equation 5-10. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \quad (\Omega)$$

Equation 5-11. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \quad \text{(pF/ft)}$$

Equation 5-12. Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \quad \text{(nH/ft)}$$

Symbols for Equation 5-5 through Equation 5-12:

- S_0 is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.
- $S_{0\ MICROSTRIP}$ and $S_{0\ STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.
- Z_0 is the intrinsic impedance of the line in Ω and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.
- C_0 is the distributed trace capacitance of the network in pF/ft.
- L_0 is the distributed trace inductance of the network in nH/ft.
- C_D is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.
- S_{EFF} and Z_{EFF} are the effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

5.3.2 Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

The effective line impedance (Z_{EFF}) is recommended to be 60 Ω ±15%, where Z_{EFF} is defined by Equation 5-10.

5.3.3 Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

5.3.3.1 Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used as an "AC ground" reference for traces to control trace impedance on the board, then the plane needs to be AC coupled to the system ground plane. This method may require more total layers in the PCB than other methods. A 1-ounce/ft^2 thick copper is recommended for all power and reference planes.

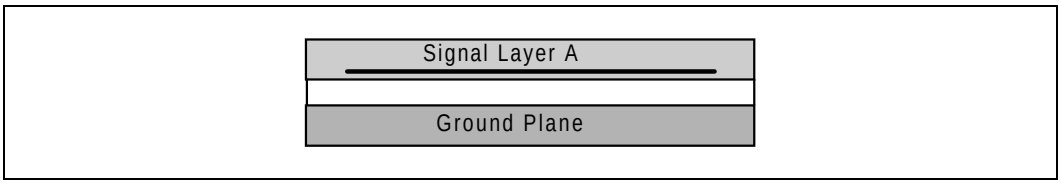
A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also

change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

5.3.3.2 Reference Planes and PCB Stackup

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 5-6 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 5-6. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 5-7). Figure 5-8 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 5-7. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 5-7. Layer Switch with One Reference Plane

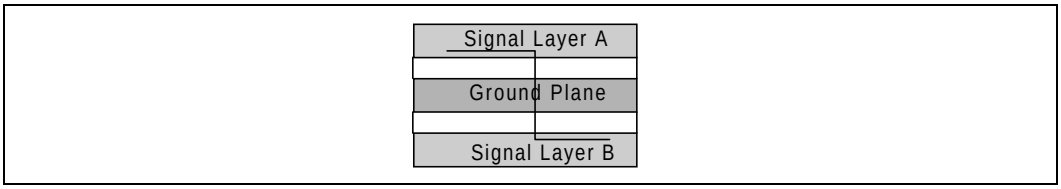
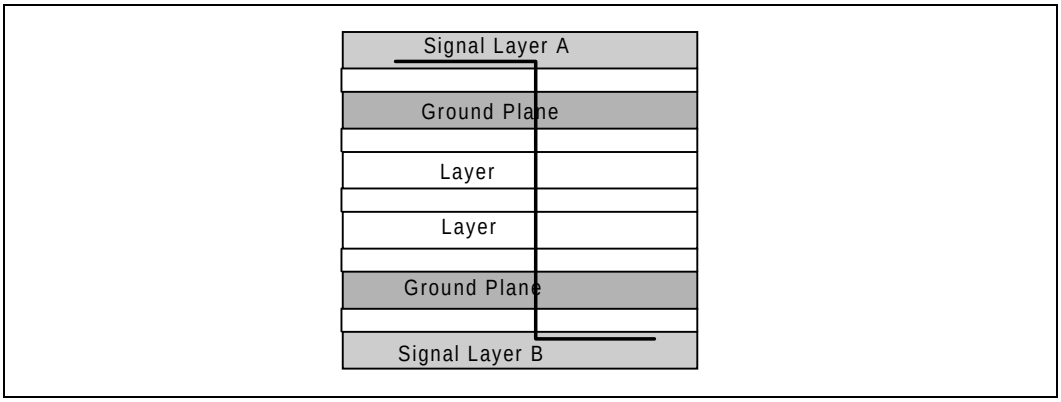


Figure 5-8. Layer Switch with Multiple Reference Planes (same type)



When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in Figure 5-9 and Figure 5-10. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 5-9. Layer Switch with Multiple Reference Planes

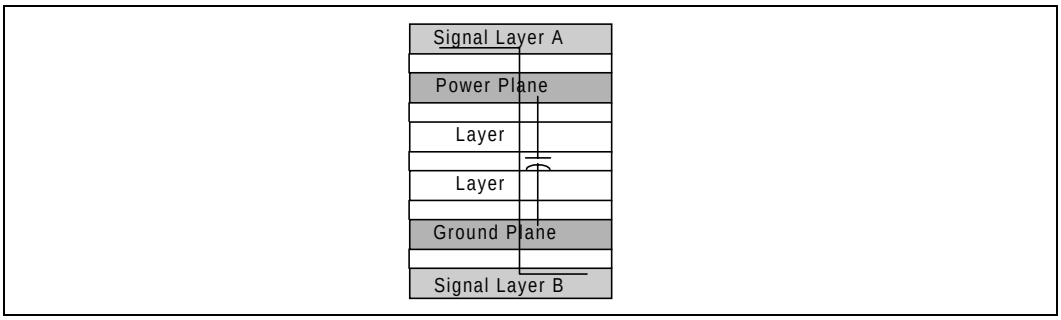
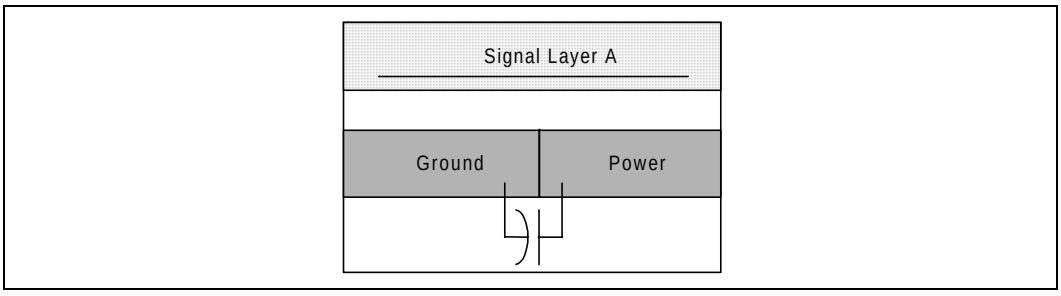


Figure 5-10. One Layer with Multiple Reference Planes



5.3.3.3 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across VCC_{CORE} and ground at the SC242 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 82810E GMCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

5.3.3.4 SC242 Connector

Intel studies indicate that the use of thermal reliefs on the connector pin layout pattern (especially ground pins) should be minimized. Such reliefs (cartwheels or wagon-wheels) increase the net ground inductance and reduce the integrity of the ground plane to which many signals are referenced. Increased ground inductance has been shown to aggravate SSO effects. Also, the anti-pad diameters (clearance holes in the planes) for the signal pins should be minimized since large anti-pads also reduce the integrity of the ground plane and increase inductance.

Some additional layout and EMI-reduction guidelines regarding the SC242 connector follow:

- Extend power/ground planes up to the SC242 connector pins.
- Extend the reference planes for AGTL+ and other controlled-impedance signals up to the SC242 connector pins.
- Minimize or remove thermal reliefs on power/ground pins.
- Route V_{TT} power with the widest signal trace or mini-plane as possible. Place decoupling caps across V_{TT} and ground in the vicinity of the connector pins.
- Use a ground plane under the principal component side of the baseboard (and secondary side if it contains active components).
- Distribute decoupling capacitors across power and ground pins evenly around the connector (less than 0.5 inch spacing) on the primary and secondary sides.
- Minimize serpentine traces on outer layers.

5.3.4 Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor's datasheet specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).
- Maintain consistent impedance for the clock traces.
  - — Minimize the number of vias in each trace.
  - — Minimize the number of different trace layers used to route the clocks.
  - — Keep other traces away from clock traces.
- Lump the loads **at the end** of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length and parallel ground trace for the **total length of each** clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace has lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

5.4 Definitions of Flight Time Measurements/ Corrections and Signal Quality

Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal Quality is defined by four parameters: Overshoot, Undershoot, Settling Limit, and Ringback. Timings are measured at the pins of the driver and receiver, while signal integrity is observed at the receiver chip pad. When signal integrity at the pad violates the following guidelines and adjustments need to be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been observed at the package pin, usually with a small timing error penalty.

5.4.1 V_{REF} Guardband

To account for noise sources that may affect the way an AGTL+ signal becomes valid at a receiver, V_{REF} is shifted by ΔV_{REF} for measuring minimum and maximum flight times. The V_{REF} Guardband region is bounded by V_{REF}-ΔV_{REF} and V_{REF}+$\Delta V_{REF.}$ ΔV_{REF} has a value of 100 mV, which accounts for the following noise sources:

- Motherboard coupling
- V_{TT} noise
- V_{REF} noise

5.4.2 Ringback Levels

The example topology covered in this guideline assumes ringback tolerance allowed to within 200 mV of 2/3 V_{TT}. Since V_{TT} is specified with approximate total ±11% tolerance, this implies a 2/3 V_{TT} (V_{REF}) range from approximately 0.89 V to 1.11 V. This places the absolute ringback limits at:

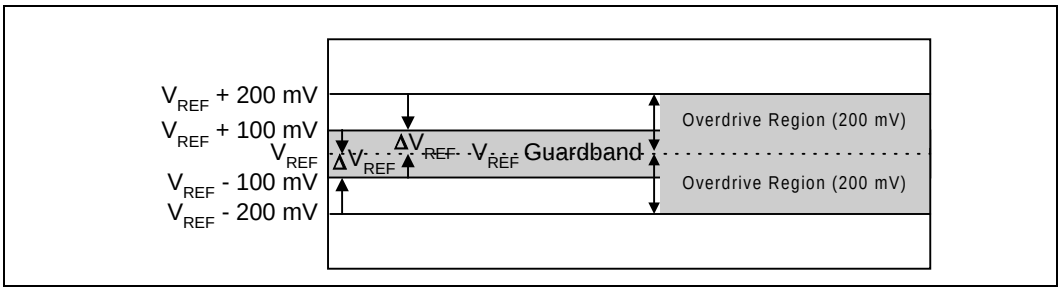
- 1.3 V (1.1 V + 200 mV) for rising edge ringback
- 0.69 V (0.89 V – 200 mV) for falling edge ringback

A violation of these ringback limits requires flight time correction as documented in the *Intel® Pentium® II Processor Developer's Manual*.

5.4.3 Overdrive Region

The overdrive region is the voltage range, at a receiver, from V_{REF} to V_{REF} + 200 mV for a low-to-high going signal and V_{REF} to V_{REF} - 200 mV for a high-to-low going signal. The overdrive regions encompass the V_{REF} Guardband. So, when V_{REF} is shifted by ΔV_{REF} for timing measurements, the overdrive region **does not** shift by ΔV_{REF}. Figure 5-11 depicts this relationship. Corrections for edge rate and ringback are documented in the *Intel® Pentium® II Processor Developer's Manual*. However, there is an exception to the documented correction method. The *Intel® Pentium® II Processor Developer's Manual* states that extrapolations should be made from the last crossing of the overdrive region back to V_{REF}. Simulations performed on this topology should extrapolate back to the appropriate V_{REF} Guardband boundary, and not V_{REF}. So, for maximum rising edge correction, extrapolate back to V_{REF} + ΔV_{REF}. For maximum falling edge corrections, extrapolate back to V_{REF} - ΔV_{REF}.

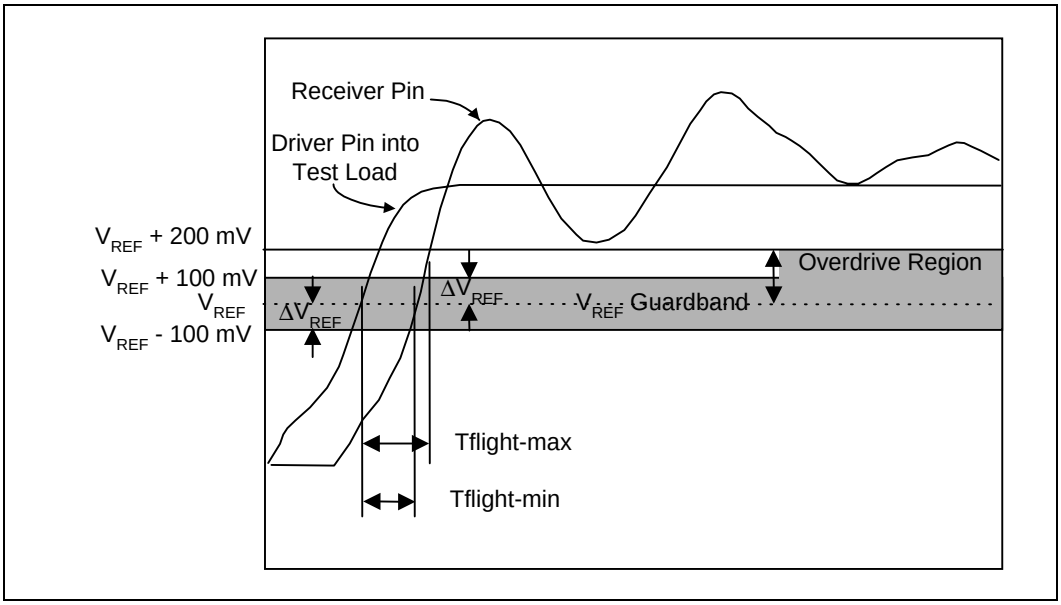
Figure 5-11. Overdrive Region and V_{REF} Guardband



5.4.4 Flight Time Definition and Measurement

Timing measurements consist of minimum and maximum flight times to take into account that devices can turn on or off anywhere in a V_{REF} Guardband region. This region is bounded by V_{REF}-ΔV_{REF} and V_{REF}+ΔV_{REF}. The minimum flight time for a rising edge is measured from the time the driver crosses V_{REF} when terminated to a test load, to the time when the signal first crosses V_{REF}-ΔV_{REF} at the receiver (see Figure 5-12). Maximum flight time is measured to the point where the signal first crosses V_{REF}+ΔV_{REF}, assuming that ringback, edge rate, and monotonicity criteria are met. Similarly, minimum flight time measurements for a falling edge are taken at the V_{REF}+ΔV_{REF} crossing and maximum flight time is taken at the V_{REF}-ΔV_{REF} crossing.

Figure 5-12. Rising Edge Flight Time Measurement



5.5 Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.



6

Clocking

Clocking 6

6.1 Clock Generation

There is only one clock generator component required in an Intel® 810E Chipset system. The CK810E clock chip is pin compatible with the CK810E clock chip, which comes in a single 56-pin SSOP package.

There is one pin function change in the CK810E relative to the CK810, the REFCLK Reset Strap:

Table 6-1. REFCLK Reset Strap for 810 vs. 810E

At Reset	APIC Clock Strap	System Bus Freq Select (SEL1)
After reset	14 MHz Clock	14 MHz Clock
Reset default	Internal Pullup for 33 MHz APIC Clock Populate External 10 KΩ Resistor to Ground for 16 MHz	Internal Pulldown for 66 MHz or 100 MHz Bus Frequency Select (SEL0) External Drive to 1 to Select 133 MHz System Bus

The CK810E is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the CK810E device requires both 3.3V and 2.5V. These power supplies should be as clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines. The CK810E provides the following clock frequencies.

Table 6-2. Intel® 810E Chipset Clocks

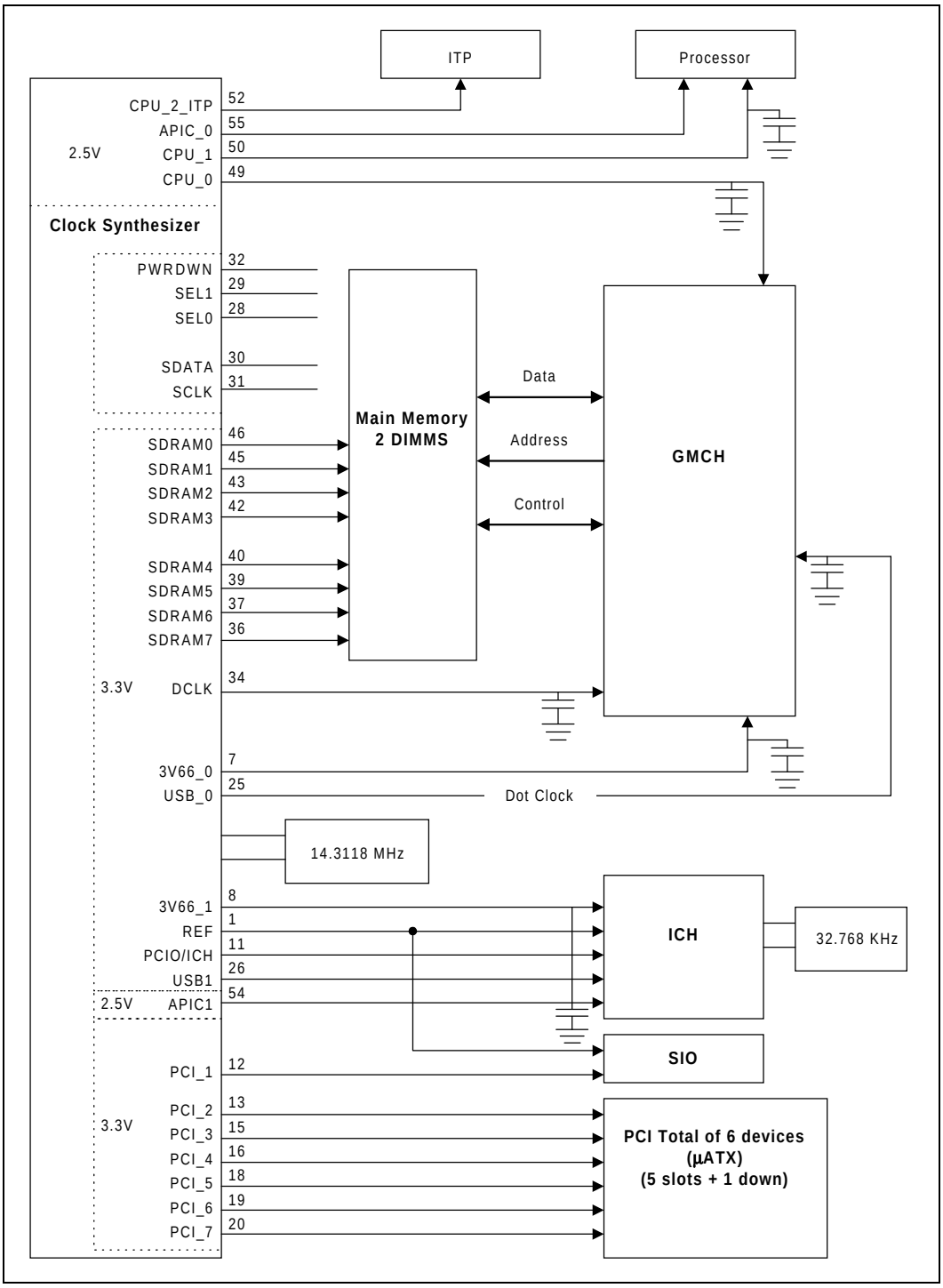
Number	Clock	Frequency
3	CPU Clocks	66/100/133 MHz
9	SDRAM Clocks	100 MHz
8	PCI Clocks	33 MHz
2	APIC Clocks	16.67/33 MHz
2	48 MHz Clocks	48 MHz
2	3V66 MHz Clocks	66 MHz
1	REF Clock	14.31818 MHz

Features (56 Pin SSOP Package)

- 3 copies of processor Clock 66/100/133 MHz (2.5V) [CPU, GMCH, ITP]
- 9 copies of 100 MHz (all the time) SDRAM Clock (3.3V) [SDRAM[0:7], DClk]
- 8 copies of PCI Clock (33 MHz) (3.3V)
- 2 copies of APIC Clock @16.67 MHz or 33 MHz, synchronous to CPU Clock (2.5V)
- 2 copy of 48 MHz Clock (3.3V) [Non SSC]
- 2 copies of 3V66 MHz Clock (3.3V)
- 1 copy of REF Clock @14.31818 MHz (3.3V) also used as input strap to determine APIC frequency
- 66/100/133 MHz CPU operation (selectable at power up only)
- Ref. 14.31818 MHz Xtal Oscillator Input
- Power Down Pin
- Spread Spectrum Support
- I^2C Support for turning off unused clocks

6.2 Clock Architecture

Figure 6-1. Intel® 810E Chipset Clock Architecture



6.3 Clock Routing Guidelines

Table 6-3 shows the group skew and jitter limits.

Table 6-3. Group Skew and Jitter Limits at the Pins of the Clock Chip

Signal Group	Pin-Pin Skew	Cycle-Cycle Jitter	Nominal Vdd	Skew, Jitter Measure Point
CPU	175 pS	250 pS	2.5V	1.25V
SDRAM	250 pS	250 pS	3.3V	1.50V
APIC	250 pS	500 pS	2.5V	1.25V
48 MHz	250 pS	500 pS	3.3V	1.50V
3V66	175 pS	500 pS	3.3V	1.50V
PCI	500 pS	500 pS	3.3V	1.50V
REF	N/A	1000 pS	3.3V	1.50V

Table 6-4 shows the Signal Group and Resistor Tolerance.

Table 6-4. Signal Group and Resistor

Signal Group	Resistor
CPU	33 ohm ± 5%
SDRAM	22 ohm ± 5%
DCLK	33 ohm ± 5%
3V66	22 ohm ± 5%
PCI	33 ohm ± 5%
TCLK	22 ohm ± 5%
OCLK/RCLK	33 ohm ± 5%
48 MHz	33 ohm ± 5%
APIC	33 ohm ± 5%
REF	10 ohm ± 5%

Table 6-5 shows the layout dimensions for the clock routing.

Note: All the clock signals must be routed on the same layer which reference to a ground plane.

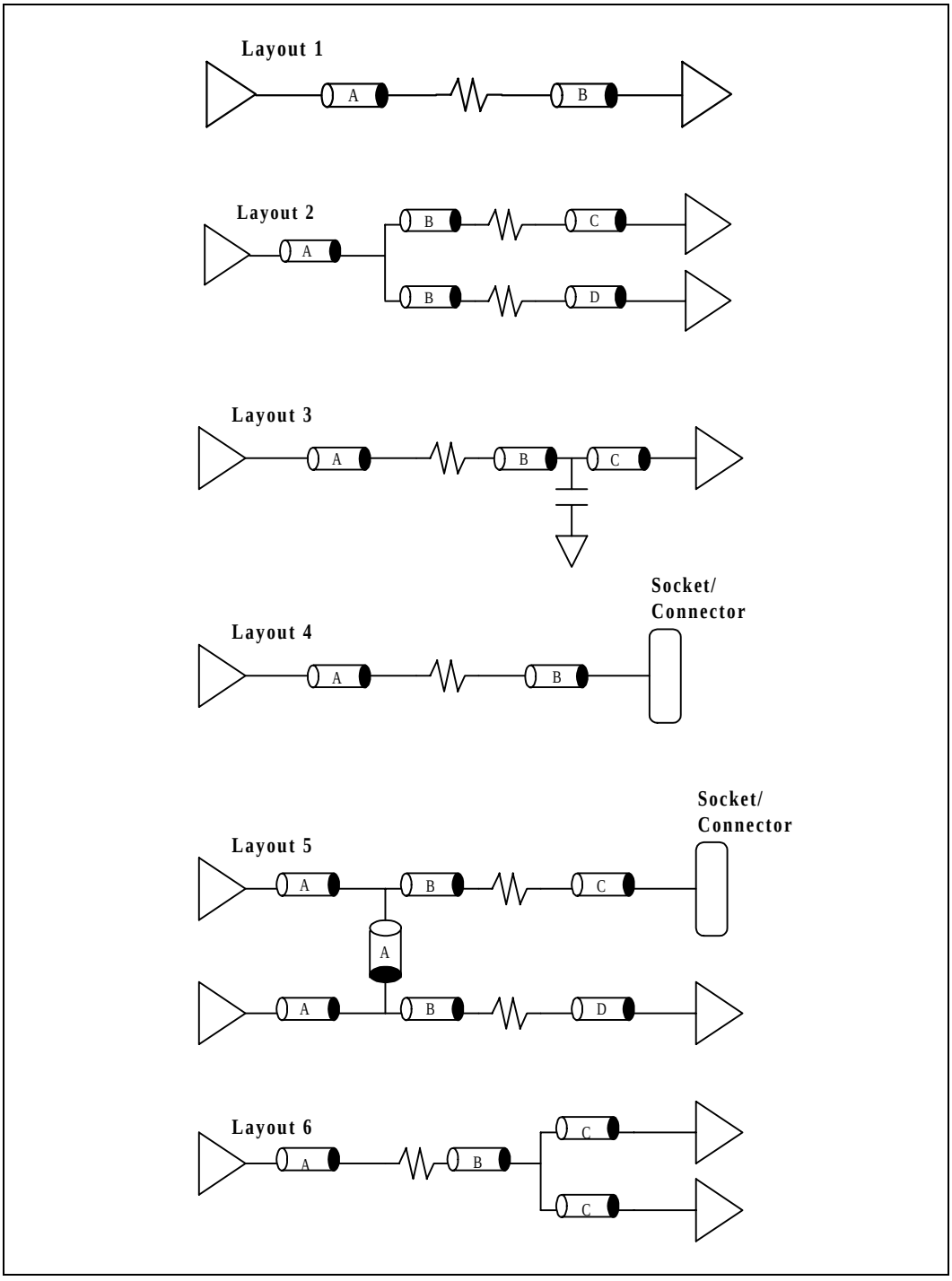
Table 6-5. Layout Dimensions

Group	Receiver	Resistor	Cap	Topology	A	B	C	D
MCLK	DIMM	22 ohm	N/A	Layout 1	0.5”	X	N/A	N/A
CPU Slot1 100/133MHz	Segment C => SEPP Segment D => GMCH	33 ohm	N/A	Layout 5	0.1”	0.5”	X+0.9"	X+7.1”
CPU FCPGA 100/133MHz	Segment C => CuMine FCPGA Segment D => GMCH	33 ohm	N/A	Layout 5	0.1”	0.5”	X+5.4"	X+7.1”
CPU Celeron 66/100MHz	Segment C => Celeron Socket Segment D => GMCH	33 ohm	N/A	Layout 5	0.1”	0.5”	X+5.4"	X+7.1”
DCLK	GMCH	33 ohm	22 pf	Layout 3	0.5”	X+3.2”	0.5”	N/A
3V66	GMCH	22 ohm	18 pF	Layout 3	0.5”	X+1.4”	0.5”	N/A
3V66	ICH	22 ohm	18 pF	Layout 3	0.5”	X+1.4”	0.5”	N/A
PCI	PCI device	33 ohm	N/A	Layout 1	0.5”	X+3.0” to X+9.3”	N/A	N/A
PCI	PCI socket	33 ohm	N/A	Layout 4	0.5”	X+0.0” to X+6.0”	N/A	N/A
PCI	ICH	33 ohm	N/A	Layout 1	0.5”	X+4.4”	N/A	N/A
TCLK	SDRAM	22 ohm	N/A	Layout 6	0.5”	1.5” to 2.5”	0.75” to 1.25”	N/A
OCLK/RCLK	GMCH	33 ohm	N/A	Layout 1	0.5”	3.25” to 3.75”	N/A	N/A
APIC	PPGA	33 ohm	N/A	Layout 4	0.5”	Y	N/A	N/A
APIC	ICH	33 ohm	N/A	Layout 1	0.5”	Y+2.4”	N/A	N/A

NOTE: W, X, Y and Z trace lengths are arbitrary. Suggested values are: X=5.0", Y=4.2".

Figure 6-2 shows the different topologies used for the clock routing guidelines.

Figure 6-2. Different Topologies for the Clock Routing Guidelines

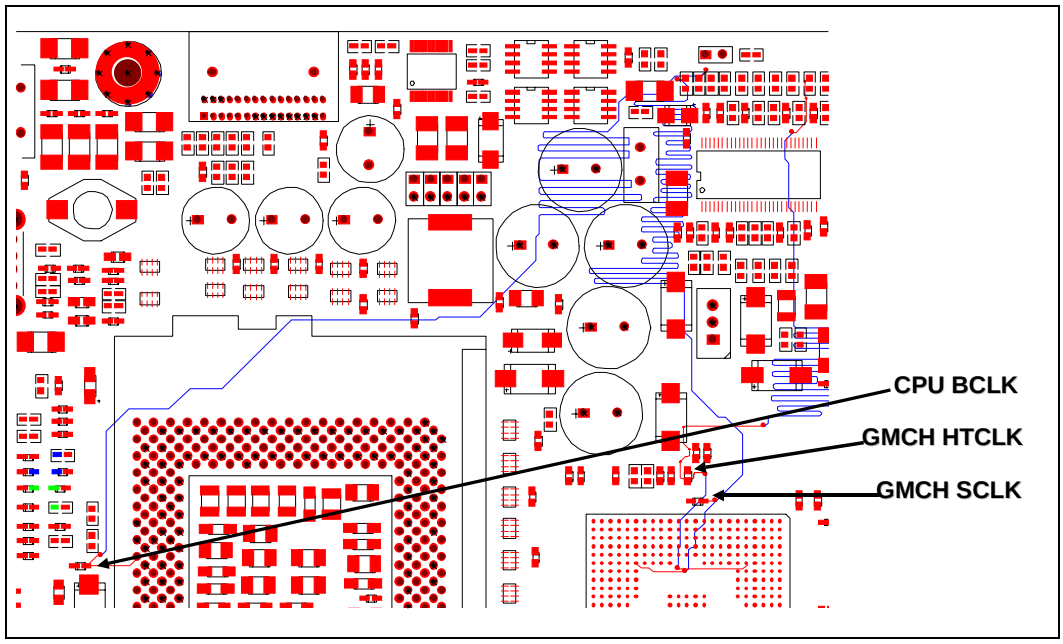


6.4 Capacitor Sites

Intel recommends 0603 package capacitor sites placed as close as possible to the clock input receivers for AC tuning for the following signal groups:

- GMCH
- Processor
- SDRAM/DCLK
- 3V66
- 3V66 to the ICH

Figure 6-3. Example of Capacitor Placement Near Clock Input Receiver



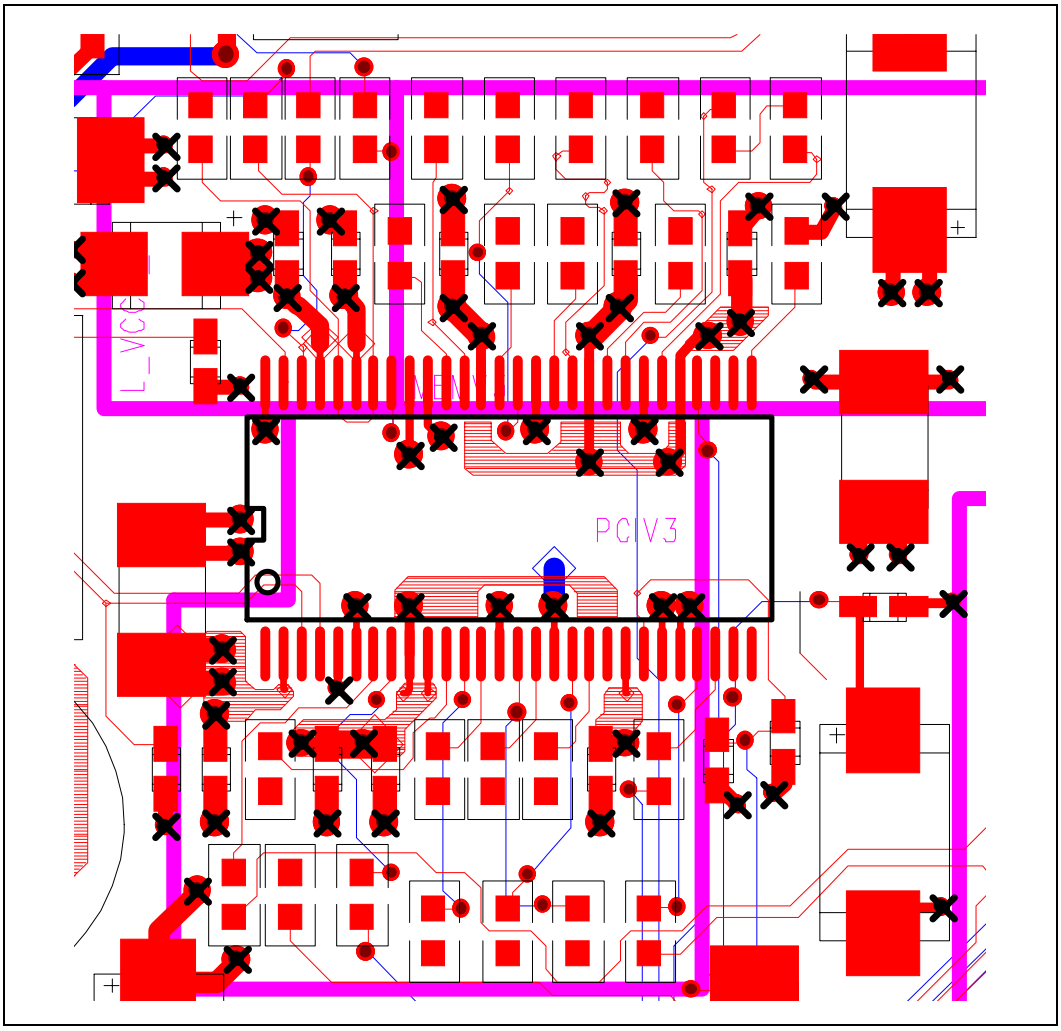
6.5 Clock Power Decoupling Guidelines

Several general layout guidelines should be followed when laying out the power planes for the CK810E clock generator.

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close to power pins as possible and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mil finished hole with a 24–26 mil path. An example power via is an 18 mil finished hole with a 33–38 mil path. For large decoupling or power planes with large current transients it is recommended to use a larger power via.

An example of clock power layout is presented in Figure 6-4.

Figure 6-4. Example of Clock Power Plane Splits and Decoupling



6.6 Clock Skew Requirements

To ensure correct system functionality, certain clocks must maintain a skew relationship to other clocks as summarized in Section 6.6.1.

6.6.1 IntraGroup Skew Limits

Clocks within each group must maintain appropriate skew relationship to each other. These requirements are summarized in Table 6-6.

Table 6-6. Clock Skew Requirements

Group Pair	Skew Limit	Measurement Point of Receiver
CPU BCLK to GMCH HTCLK	350 pS window	Pin on top of PPGA PKG GMCH Ball
GMCH SCLK to DIMM Clocks	±630 pS Referenced to GMCH SCLK	GMCH Ball DRAM Component Pin on Module
GMCH HubCLK to ICH HubCLK	575 pS window	GMCH Ball ICH Ball



7

System Design Considerations

System Design Considerations 7

7.1 Power Delivery

Power delivery terminology definitions are indicated in Section 1.1, “About This Design Guide” on page 1-1.

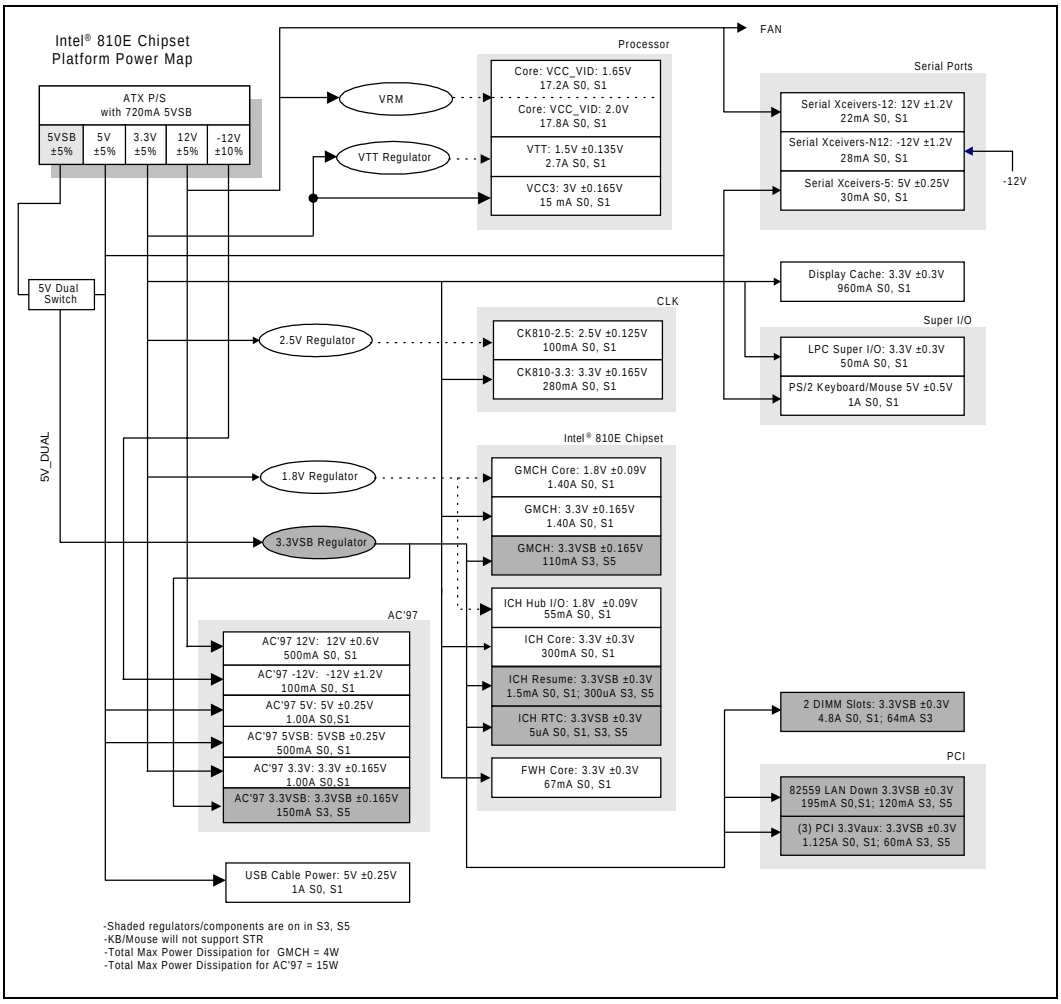
7.1.1 Intel® 810E Chipset Power Delivery

Figure 7-1 shows the power delivery architecture for an example Intel® 810E Chipset Platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3Vaux), the Intel® 82559 LAN down chip, AC’97 and optionally USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in *suspend* and in *full-power*. The power requirements should be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples to consider the effect of the change.

Figure 7-1. Intel® 810E Chipset Power Delivery Architecture



NOTE: The above current values represent the maximum sustained current draw.

Table 7-1. Intel® 810E Chipset Power Map

Voltage	Description	Voltage Lo (V)	Voltage Nom (V)	Voltage Hi (V)	Current Max (mA)	Power Max[1] (mW)	Current Max (SB) (mA)	Power Max[2] (SB) (mW)
1.5 V	Processor V_{TT}	1.365	1.5	1.635	2700	4414.5	N/A	N/A
1.8 V	ICH Hub interface I/O	1.710	1.8	1.890	55	103.95	N/A	N/A
	GMCH Core	1.710	1.8	1.890	1420	2683.8	N/A	N/A
2.0 V	processor VCC_{CORE}		2.0		17800	35600	N/A	N/A
2.5 V	CLK-2.5	2.375	2.5	2.625	100	262.5	N/A	N/A
3.3 V	processor 3.3V	3.135	3.3	3.465	15	52	N/A	N/A
3.3 V	CLK-3.3	3.135	3.3	3.465	280	970.2	N/A	N/A
	ICH Core	3.000	3.3	3.600	300	1080	N/A	N/A
	Display Cache	3.000	3.3	3.600	960	3456	N/A	N/A
	FWH Core	3.000	3.3	3.600	67	241.2	N/A	N/A
	AC'97 3.3V	3.135	3.3	3.465	1000	3465	N/A	N/A
	GMCH	3.135	3.3	3.465	330	1143.45	N/A	N/A
	Super I/O	3.000	3.3	3.600	50	180	N/A	N/A
3.3 VSB	ICH Resume	3.000	3.3	3.600	0.3	1.08	1.5	5.4
	ICH RTC	3.000	3.3	3.600	0.005	0.018	0.006	0.0216
	GMCH	3.135	3.3	3.465	N/A	N/A	110	103.95
	PCI (3 slots)	3.000	3.3	3.600	1125	4050	60	216
	82559 LAN Down	3.000	3.3	3.600	195	702	120	432
	AC'97 3.3 VSB	3.135	3.3	3.465	1000	3465	150	519.75
	2 DIMM Slots	3.000	3.3	3.600	4800	17280	64	230.4
5 V	Serial Xceivers-5	4.500	5.0	5.500	30	165	N/A	N/A
	Keyboard/Mouse	4.500	5.0	5.500	1000	5500	N/A	N/A
	AC'97 5V	4.750	5.0	5.250	1000	5250	N/A	N/A
	USB	4.750	5.0	5.250	1000	5250	N/A	N/A
	AC'97 5 VSB	4.750	5.0	5.250	500	2625	N/A	N/A
12 V	AC'97 12V	11.400	12.0	12.600	500	6300	N/A	N/A
	Serial Xceivers 12V	10.800	12.0	13.200	22	290.4	N/A	N/A
-12 V	AC'97 -12V	10.800	12.0	13.200	100	1320	N/A	N/A
	Serial Xceivers -12V	10.800	12.0	13.200	28	369.6	N/A	N/A
TOTAL						**106.2 W**	**505.5 mA**	**1.79 W**

NOTES:
1. Power Max is calculated using the values from Voltage Hi and Current Max columns (V Hi x I Max).
2. Power Max (SB) is calculated using the values from Voltage Hi and Current Max (SB) columns (V Hi x I Max (SB)).

In addition to the power planes provided by the ATX power supply, an *instantly available* Intel® 810E Chipset system (using *Suspend-to-RAM)* requires additional power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the Intel® 810E Chipset platform can have a *5V Dual Switch*.

5V Dual Switch

This switch powers the *5V Dual plane* from the 5V core ATX supply during *full-power* operation. During *Suspend-to-RAM,* the *5V Dual plane* will be powered from the 5V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5.0V!** There is a resistive drop through the *5V Dual Switch* that should be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the Customer Reference Board, the only device connected directly to the 5V Dual plane is the 3.3V voltage regulator (to regulate to lower voltages).

Table 7-2. Intel® 810E Chipset Voltage Regulator Specifications

Voltage	Max Current
1.5 V	2.7 A
1.8 V	1.5 A
2.5 V	0.6 A
3.3 V	7.2 A
VCC_{CORE}	15.6 A

VCC_{CORE}

This power plane is used to power the processor. Refer to the latest revisions of the following documents:

- *VRM 8.4 Rev 1.5 DC-DC Converter Design Guidelines*
- *PPGA 370 Power Delivery Guidelines*
- *AP-907: Intel®Pentium® III Power Distribution Guidelines*

Note: This regulator is required in ALL designs.

V_{TT}

This power plane is used to power the AGTL+ termination resistors. Refer to the latest revisions of:

- *Intel® Pentium™ III Processor Datasheet*

Note: This regulator is required in ALL designs.

1.8V

The 1.8V plane powers the GMCH core, the ICH Hub interface I/O, and digital video out. This voltage is obtained from using a 1.8V voltage regulator that regulates the voltage from the 3.3V power supply voltage (or the 5V power supply voltage).

Note: This regulator is required in ALL designs.

2.5V

The 2.5V plane powers the 2.5V rail of the clock synthesizer and the CMOS pullups to the processor. This voltage is obtained from using a 2.5V voltage regulator that regulates the voltage from the 3.3V power supply voltage (or the 5V power supply voltage).

Note: This regulator is required in ALL designs.

3.3VSB

The 3.3VSB plane powers the suspend well of the ICH, the ICH Real Time Clock, the AC'97 AMR connector, the 2 DIMM slots, and the PCI 3.3Vaux suspend power pins.

The 3.3Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to *EACH* card. Therefore, the total current requirement for the PCI 3.3Vaux suspend power pins is:

- *Full-power Operation:* 375 mA*number of PCI slots
- *Suspend Operation:* 375+20*(number of PCI slots – 1)

The total maximum current requirement for the 3.3VSB power plane (as well as the 3.3V regulator) is 7.12 A.

Note: This regulator is required in ALL designs.

7.1.2 LED Indicator for S0-S5 States

Although not required by the ACPI Specification, Intel recommends that an on-board LED be implemented that informs the user that the system is in a full-on or a sleep state (as opposed to a mechanical off state). In general, depending on the particular implementation, it may not be safe to add/remove hardware to the system while the system is in an S5 state. Since the S5 state may closely resemble the mechanical off state, (i.e., display blank, fans off, no noise, etc.) this LED indicator, when lit, lets the user know that it is NOT safe to add/remove hardware to the system. Implementation of this LED indicator may help prevent hardware damage to the system when a user is changing hardware. This may be implemented by connecting an LED to one of the auxiliary power supplies.

7.2 Decoupling Guidelines

7.2.1 Vcc_{CORE} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep an interconnect resistance from the regulator (or VRM pins) to the Socket pins of less than 0.3m ohm. This can be accomplished by keeping a maximum distance of 1.0 inches between the regulator output and Socket Vcc pins. The recommended Vcc_{CORE} interconnect is a 2.0 inch wide (the width of the VRM 8.2 connector) by 1.0 inch long (maximum distance between the 370-pin socket and the VRM connector) plane segment with a standard 1-ounce plating. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM) defined in the *VRM 8.2 DC-DC Converter Design Guidelines*. The Vcc_{CORE} supply should be capable of delivering a recommended minimum dI_{CCCORE}/dt while maintaining the required tolerances.

Adequate decoupling capacitance should be placed near the power pins of the Intel® Celeron™ processor PPGA. In order to obtain optimal performance Intel recommends using 10 or more 4.7 uF 1206-style capacitors and 19 or more 1.0 uF 0805-style capacitors when using a conventional Voltage Regulator Module. Inductance should be reduced by connecting capacitors directly to the Vcc_{CORE} and Vss planes with minimal trace length between the component pads and

vias to the plane. Be sure to include the effects of board inductance within the simulation. Also, when choosing the capacitors to use, keep in mind the operating temperatures that will be seen and the rated tolerance.

Bulk capacitance with a low Effective Series Resistance (ESR) should also be placed near the Intel® Celeron™ processor PPGA to handle changes in average current between the low-power and normal operating states. About 9000 uF of capacitance with an ESR of 5m ohm makes a good starting point for simulations, although more capacitance may be needed to bring the ESR down to this level due to the current technology in the industry. Voltage Regulator Modules already contain this bulk capacitance. Be sure to determine what is available on the market before choosing parameters for the models. Also, include power supply response time and cable inductance in a full simulation.

The Intel® Celeron™ processor PPGA does not contain high frequency decoupling capacitance on the processor package. High frequency decoupling and bulk decoupling should be provided for by the system motherboard for proper AGTL+ bus operation.

Although the system bus receives power external to the processor, this power supply will also require the same diligent decoupling methodologies as the processor. Note that the existence of external power entering through the I/O buffers causes Vss current to be higher than the Vcc_{CORE} current. For more information the following documents are recommended:

- *Pentium® III Processor AGTL+ Guidelines*
- *Pentium® III Processor Power Distribution Guideline*
- *Pentium® III Processor Developer's Manual*

7.2.2 Phase Lock Loop (PLL) Decoupling

Isolated analog decoupling is required for the internal PLL. This should be a 22 µF ±20% capacitor and a 22 µH ±30% inductor. The capacitor should be across the PLL1 and PLL2 pins of the processor. The inductor should be connected from PLL1 to Vcc_{CORE}.

7.2.3 GMCH Decoupling Guidelines

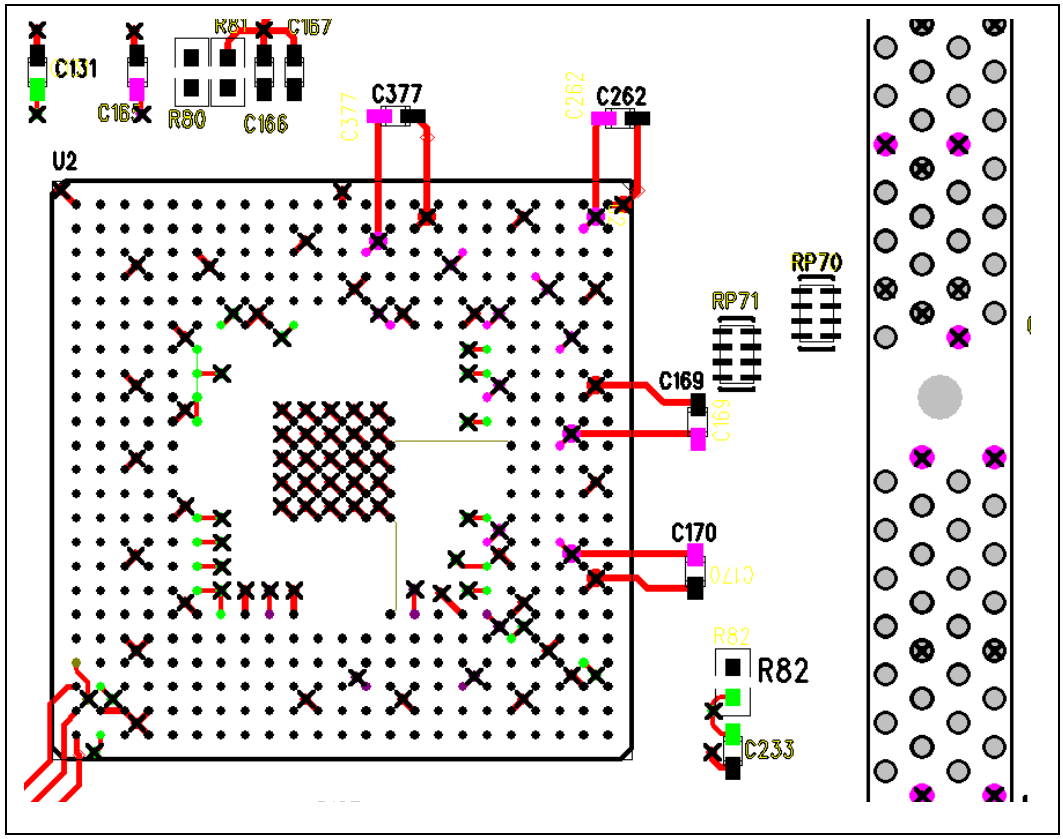
GMCH Vsus 3.3V (3.3V Standby) Power Plane Decoupling

- 3.3V Droop Spec.
  - — Worse case droop on 3.3V plane must not go below 2.5 V.
  - — *Droop below the minimum Vcc of 3.135 V must not occur for a period greater than 2ns.*
- Place four 0.01 µF decoupling capacitors as close as possible to GMCH.
  - — Trace from cap pad to via < 500 mils (Ideal = 300 mils).
  - — Trace width at least 15 mils.
- Use power vias (multiple if possible).
  - — Power via example: 18 mil drill, 33–38 mil width.
- Place capacitors orientation such that flight time will be minimized.
  - — Vias between GMCH ball and cap pad (see Figure 7-2).

Power Plane Layout

- Make the power planes as square as possible with no sharp corners.
- Avoid crossing traces over multiple power planes.

Figure 7-2. GMCH Power Plane Decoupling



7.3 Thermal Design Power

Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the GMCH component is 4.0 W.

7.4 Power Sequencing

This section shows the timings between various signals during different power state transitions.

Figure 7-3. G3-S0 Transistion

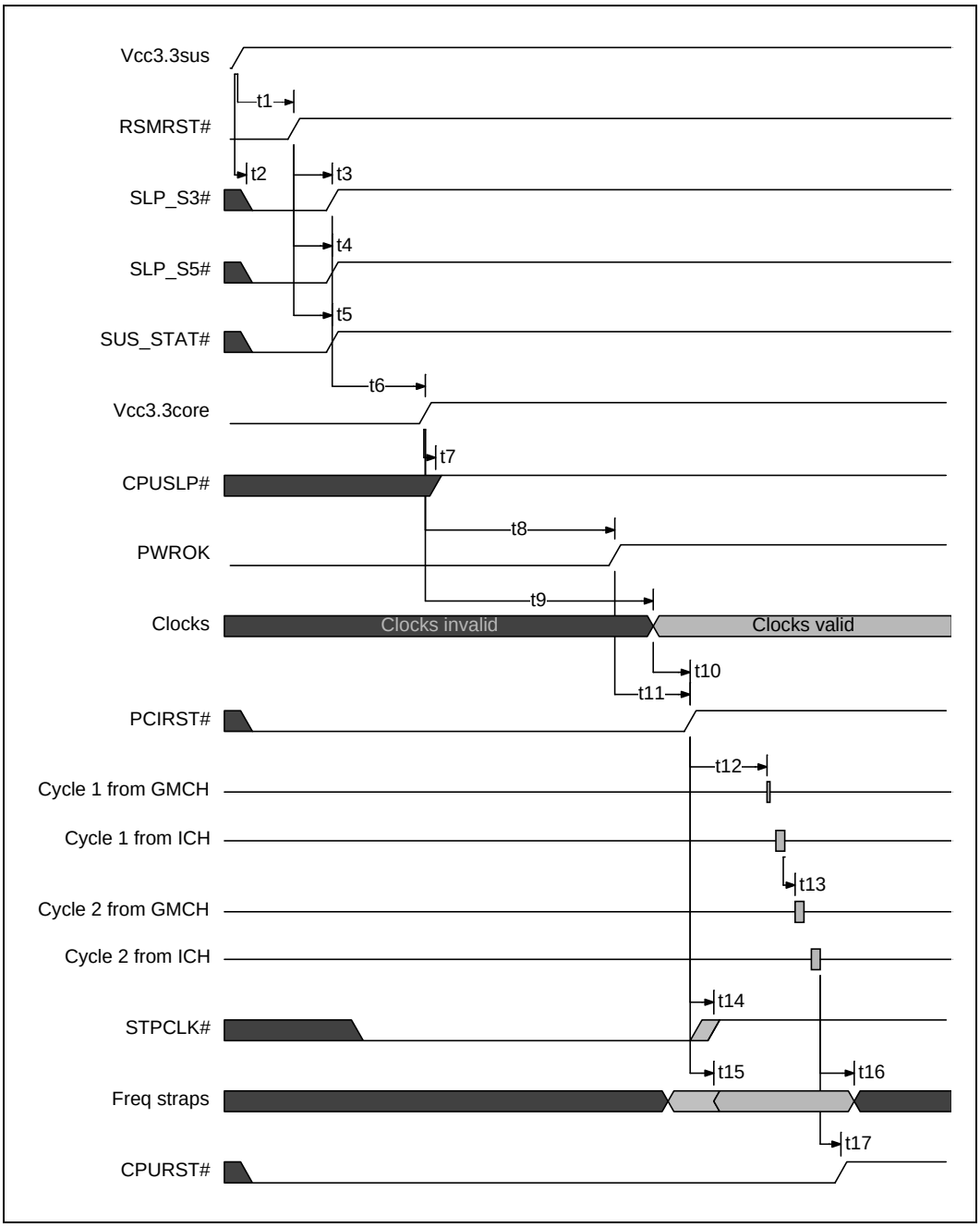


Figure 7-4. S0-S3-S0 Transition

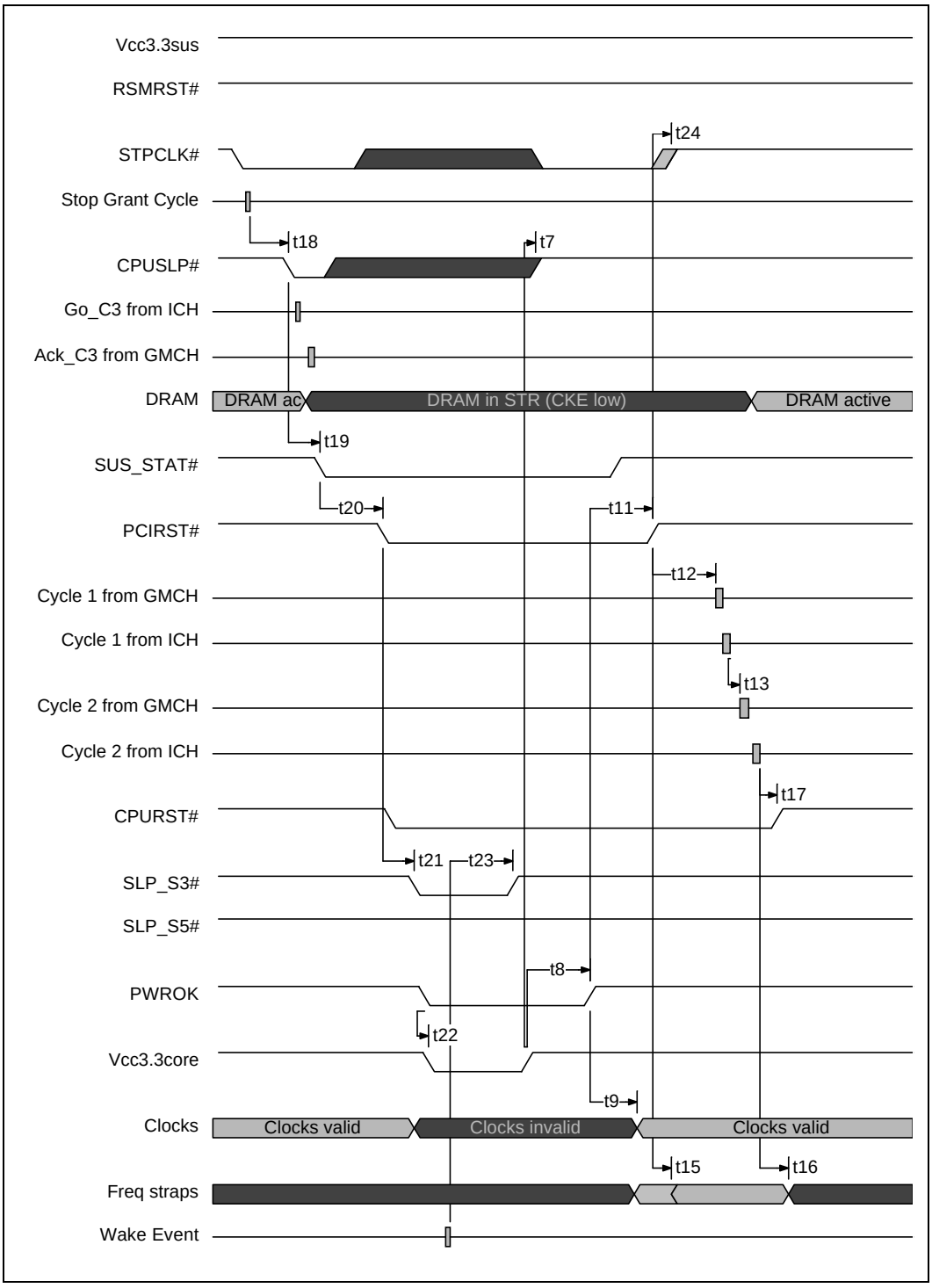


Figure 7-5. S0-S5-S0 Transition

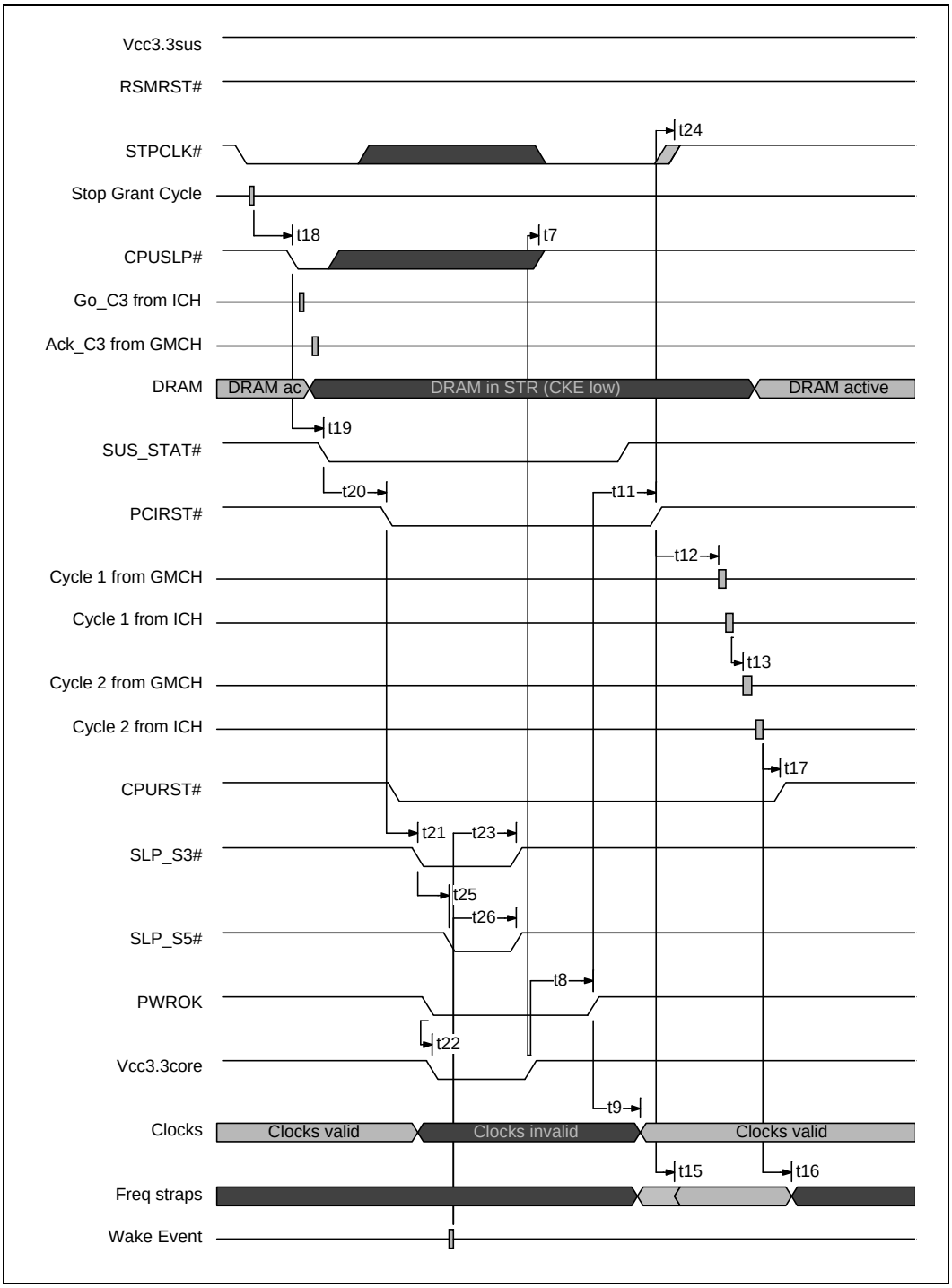


Table 7-3. Power Sequencing Timing Definitions

Symbol	Parameter	Min.	Max.	Units
t1	VccSUS Good to RSMRST# inactive	1	25	ms
t2	VccSUS Good to SLP_S3#, SLP_S5#, and PCIRST# active		50	ns
t3	RSMRST# inactive to SLP_S3# inactive	1	4	RTC clocks
t4	RSMRST# inactive to SLP_S5# inactive	1	4	RTC clocks
t5	RSMRST# inactive to SUS_STAT# inactive	1	4	RTC clocks
t6	SLP_S3#, SLP_S5#, SUS_STAT# inactive to Vcc3.3core good	*	*	
t7	Vcc3.3core good to CPUSLP# inactive		50	ns
t8	Vcc3.3core good to PWROK active	*	*	
t9	Vcc3.3core good to clocks valid	*	*	
t10	Clocks valid to PCIRST# inactive	500		us
t11	PWROK active to PCIRST# inactive	.9	1.1	ms
t12	PCIRST# inactive to Cycle 1 from GMCH		1	ms
t13	Cycle 1 from ICH to Cycle 2 from GMCH		60	ns
t14	PCIRST# inactive to STPCLK de-assertion	1	4	PCI clocks
t15	PCIRST# to frequency straps valid	-4	4	PCI clocks
t16	Cycle 2 from ICH to frequency straps invalid		180	ns
t17	Cycle 2 from ICH to CPURST# inactive		110	ns
t18	Stop Grant Cycle to CPUSLP# active		8	PCI clocks
t19	CPUSLP# active to SUS_STAT# active		1	RTC clock
t20	SUS_STAT# active to PCIRST# active	2	3	RTC clocks
t21	PCIRST# active to SLP_S3# active	1	2	RTC clocks
t22	PWROK inactive to Vcc3.3core not good	20		ns
t23	Wake event to SLP_S3# inactive	2	3	RTC clocks
t24	PCIRST# inactive to STPCLK# inactive	1	4	PCI clocks
t25	SLP_S3# active to SLP_S5# active	1	2	RTC clocks
t26	SLP_S5# inactive to SLP_S3# inactive	2	3	RTC clocks

NOTE: * This value is board dependent.



8

Design Checklist

Design Checklist 8

8.1 Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel® 810E Chipset. This is not a complete list and does not guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the Design Guide for more detailed instructions on designing a motherboard.

8.1.1 Design Checklist Summary

The following tables provide design considerations for the various portions of a design. Each table describes one of those portions, and is titled accordingly. Contact your Intel Field Representative for questions or issues regarding interpretation of the information contained in these tables.

Table 8-1. AGTL+ Connectivity Checklist for 370-Pin Socket Processors

CPU Pin	I/O	Comments
A[35:3]# [1]	I/O	Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
ADS# [1]	I/O	Connect to GMCH.
AERR#	I/O	Leave as No Connect (not supported by chipset).
AP[1:0]#	I/O	Leave as No Connect (not supported by chipset).
BERR#	I/O	Leave as No Connect (not supported by chipset).
BINIT#	I/O	Leave as No Connect (not supported by chipset).
BNR# [1]	I/O	Connect to GMCH.
BP[3:2]#	I/O	Leave as No Connect.
BPM[1:0]	I/O	Leave as No Connect.
BPRI# [1]	I	Connect to GMCH.
BREQ[0]# (BR0#)	I/O	10Ω pulldown resistor to ground.
D[63:0]# [1]	I/O	Connect to GMCH.
DBSY# [1]	I/O	Connect to GMCH.
DEFER# [1]	I	Connect to GMCH.
DEP[7:0]#	I/O	Leave as No Connect (not supported by chipset).
DRDY# [1]	I/O	Connect to GMCH.
HIT# [1]	I/O	Connect to GMCH.
HITM# [1]	I/O	Connect to GMCH.
LOCK# [1]	I/O	Connect to GMCH.
REQ[4:0]# [1]	I/O	Connect to GMCH.
RESET#	I	56Ω pullup resistor to Vtt, connect to GMCH, 240Ω series resistor to ITP.
RESET2# [2]	I	Driven by same signal as RESET#.
RP#	I/O	Leave as No Connect (not supported by chipset).
RS[2:0]#	I	Connect to GMCH.
RSP#	I	Leave as No Connect (not supported by chipset).
TRDY# [1]	I	Connect to GMCH.

NOTES:
1. For Intel® Celeron™ (PPGA package) processor electrical compatibility, the motherboard must include AGTL+ termination resistors. If the Intel® Celeron™ processor is not supported, AGTL+ termination is provided by the Intel® Pentium® III processor (**except RESET#**).
2. If the Intel® Celeron™ processor is not supported by the motherboard, then RTTCTRL is pulled down with a 56Ω resistor and RESET2# is grounded.

Table 8-2. CMOS Connectivity Checklist for 370-Pin Socket Processors

CPU Pin	I/O	Comments
A20M#	I	150Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
FERR#	O	150Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
FLUSH#	I	150Ω pullup resistor to VCC_{CMOS} (not used by chipset).
IERR#	O	150 Ω pullup resistor to VCC_{CMOS} if tied to custom logic or leave as No Connect (not used by chipset).
IGNNE#	I	150 Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
INIT#	I	150 Ω pullup resistor to VCC_{CMOS} / Connect to ICH & FWH.
LINT0/INTR	I	150 Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
LINT1/NMI	I	150 Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
PICD[1:0]	I/O	150 Ω pullup resistor to VCC_{CMOS} / Connect to ICH.
PREQ#	O	~200–330 Ω pullup resistor to VCC_{CMOS} / Connect to ITP.
PWRGOOD	I	150–330 Ω pull-up to 2.5V, output from the PWRGOOD logic.
SLP#	I	150 Ω pull-up to VCC_{CMOS} / Connect to ICH.
SMI#	I	150 Ω pull-up to VCC_{CMOS} / Connect to ICH.
STPCLK#	I	150 Ω pull-up to VCC_{CMOS} / Connect to ICH.
THERMTRIP#	O	150 Ω pullup resistor to VCC_{CMOS} and connect to power off logic, or leave as No Connect.

Table 8-3. TAP Checklist for a 370-Pin Socket Processor [3,4]

CPU Pin	I/O	Comments
TCK	I	1 KΩ pullup resistor to VCC_{CMOS} / 47 Ω series resistor to ITP.
TDI	I	~200–330 Ω pullup resistor to VCC_{CMOS} / Connect to ITP.
TDO	O	150 Ω pullup resistor to VCC_{CMOS} / Connect to ITP.
TMS	I	1 KΩ pullup resistor to VCC_{CMOS} / 47 Ω series resistor to ITP.
TRST#	I	~680 Ω pulldown resistor to ground / Connect to ITP.
PRDY#	I	150 Ω pullup resistor to Vtt / 240 Ω series resistor to ITP.

NOTES:
1. The ITP connector is different than the one previously specified for other Intel IA-32 processors. It is the female counterpart to the previously specified connector and is specifically for use with processors utilizing 1.5V CMOS TAP I/O signals.
2. The Intel® Pentium® III processor requires an ITP with a 1.5V tolerant buffer board. Previous ITPs are designed to work higher voltages and may damage the processor if they are connected to an Intel® Pentium® III FC-PGA processor.

Table 8-4. Miscellaneous Checklist for 370-Pin Socket Processors

CPU Pin	I/O	Comments
BCLK	I	Connect to clock generator / 22-33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0	I/O	**Case 1**, 66/100/133MHz support: 1 KΩ pullup resistor to 3.3V, connect to CK810E SEL0 input, connect to GMCH LMD29 pin via 10 KΩ series resistor. **Case 2**, 100/133MHz support: 1 KΩ pullup resistor to 3.3V, connect to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD.
BSEL1	I/O	1 KΩ pullup resistor to 2.5V, connect to CK810E REF pin via 10KΩ series resistor, connect to GMCH LMD13 pin via 10 KΩ series resistor.
CLKREF	I	Connect to divider on VCC_2.5 or VCC_3.3 to create 1.25V reference with a 4.7 uF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. **Do not use VTT as source voltage for this reference!**
CPUPRES#		Tie to ground, leave as No Connect, or could be connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1K–10KΩ pullup resistor to any voltage.
EDGCTRL	I	51 Ω ±5% pullup resistor to VCC_{CORE}.
PICCLK	I	Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics).
PLL1, PLL2	I	Low pass filter on VCC_{CORE} provided on motherboard. Typically a 4.7uH inductor in series with VCC_{CORE} is connected to PLL1 then through a series 33 uF capacitor to PLL2.
RTTCTRL[5] (S35)		110 Ω ±1% pulldown resistor to ground.
SLEWCTRL (E27)		110 Ω ±1% pulldown resistor to ground.
THERMDN	O	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
THERMDP	I	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
VCC_1.5	I	Connected to same voltage source as V_{TT}. Must have some high and low frequency decoupling.
VCC_2.5	I	Connected to 2.5V voltage source. Should have some high and low frequency decoupling.
VCC_{CMOS}	O	Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/LF) present.
VCC_{CORE}	I	10 ea (min) 4.7 uF in 1206 package all placed within the PGA370 socket cavity. 8 ea (min) 1 uF in 0612 package placed in the PGA370 socket cavity.
$VCORE_{DET}$ (E21)	O	220 Ω pullup resistor to 3.3V, connect to GMCH LMD27 pin via 10 KΩ series resistor.
VID[3:0]	O	Connect to on-board VR or VRM. For on-board VR, 10 KΩ pullup resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pullups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VID[4]	N/A	Connect regulator controller pin to ground (not on processor).
VREF[7:0]	I	Connect to Vref voltage divider made up of 75 and 150 ohm 1% resistors connected to Vtt. Decoupling Guidelines: 4 ea. (min) 0.1 uF in 0603 package placed within 500 mils of VREF pins.

Table 8-4. Miscellaneous Checklist for 370-Pin Socket Processors (Continued)

CPU Pin	I/O	Comments
VTT	I	Connect AH20, AK16, AL13, AL21, AN11, AN15, and G35 to 1.5V regulator. Provide high and low frequency decoupling. Decoupling Guidelines: 19 ea (min) 0.1uF in 0603 package placed within 200 mils of AGTL+ termination resistor packs (r-paks). Use one capacitor for every two (r-paks). 4 ea (min) 0.47uF in 0612 package
NO CONNECTS	N/A	The following pins must be left as no-connects: AA33, AA35, AK30, AM2, AN21, E23, F10, G37, L33, N33, N35, N37, Q33, Q35, Q37, R2, S33, S37, U35, U37, W35, X2, Y1

NOTES:
1. If the Intel® Celeron™ processor (PPGA) is not supported by the motherboard, then RTTCTRL is pulled down with a 56 Ω resistor and RESET2# is grounded.

Table 8-5. AGTL+ Connectivity Checklist for SC242 Processors

CPU Pin	I/O	Comments
A[35:3]# [1]	I/O	Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
ADS# [1]	I/O	Connect to GMCH.
AERR#	I/O	Leave as No Connect (not supported by chipset).
AP[1:0]#	I/O	Leave as No Connect (not supported by chipset).
BERR#	I/O	Leave as No Connect (not supported by chipset).
BINIT#	I/O	Leave as No Connect (not supported by chipset).
BNR# [1]	I/O	Connect to GMCH.
BP[3:2]#	I/O	Leave as No Connect.
BPM[1:0]	I/O	Leave as No Connect.
BPRI# [1]	I	Connect to GMCH.
BREQ[0]# (BR0#)	I/O	10 Ω pulldown resistor to ground.
BREQ[1]# (BR1#)	I	Leave as No Connect (not supported by chipset).
D[63:0]# [1]	I/O	Connect to GMCH.
DBSY# [1]	I/O	Connect to GMCH.
DEFER# [1]	I	Connect to GMCH.
DEP[7:0]#	I/O	Leave as No Connect (not supported by chipset).
DRDY# [1]	I/O	Connect to GMCH.
HIT# [1]	I/O	Connect to GMCH.
HITM# [1]	I/O	Connect to GMCH.
LOCK# [1]	I/O	Connect to GMCH.
REQ[4:0]# [1]	I/O	Connect to GMCH.
RESET# [1]	I	Connect to GMCH / 240 Ω series resistor to ITP.
RP#	I/O	Leave as No Connect (not supported by chipset).
RS[2:0]#	I	Connect to GMCH.
RSP#	I	Leave as No Connect (not supported by chipset).
TRDY# [1]	I	Connect to GMCH.

NOTES:
1. For SET (Single-Ended Termination) designs, no motherboard Rtt is present for AGTL+ signals.

Table 8-6. CMOS Connectivity Checklist for SC242 Processors

CPU Pin	I/O	Comments
A20M#	I	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
FERR#	O	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
FLUSH#	I	150 Ω pullup resistor to VCC_2.5 (not used by chipset).
IERR#	O	150 Ω pullup resistor to VCC_2.5 if tied to custom logic or leave as No Connect (not used by chipset).
IGNNE#	I	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
INIT#	I	150 Ω pullup resistor to VCC_2.5 / Connect to ICH & FWH.
LINT0/INTR	I	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
LINT1/NMI	I	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
PICD[1:0]	I/O	150 Ω pullup resistor to VCC_2.5 / Connect to ICH.
PREQ#	O	~200-330 Ω pullup resistor to VCC_2.5 / Connect to ITP.
PWRGOOD	I	150-330 Ω pull-up to 2.5V, output from the PWRGOOD logic.
SLP#	I	150 Ω pull-up to VCC_2.5 / Connect to ICH.
SMI#	I	150 Ω pull-up to VCC_2.5 / Connect to ICH.
STPCLK#	I	150 Ω pull-up to VCC_2.5 / Connect to ICH.
THERMTRIP#	O	150 Ω pullup resistor to VCC_2.5 and connect to power off logic, or leave as No Connect.

Table 8-7. TAP Checklist for SC242 Processors

CPU Pin	I/O	Comments
TCK	I	1K Ω pullup resistor to VCC_2.5 / 47 Ω series resistor to ITP.
TDI	I	~200-330 Ω pullup resistor to VCC_2.5 / Connect to ITP.
TDO	O	150 Ω pullup resistor to VCC_2.5 / Connect to ITP.
TMS	I	1K Ω pullup resistor to VCC_2.5 / 47 Ω series resistor to ITP.
TRST#	I	~680 Ω pulldown resistor to ground / Connect to ITP.
PRDY#	I	150 Ω pullup resistor to Vtt / 240 Ω series resistor to ITP.

Table 8-8. Miscellaneous Checklist for SC242 Processors

CPU Pin	I/O	Comments
BCLK	I	Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0	I/O	**Case 1**, 66/100/133 MHz support: 220 Ω pullup resistor to 3.3V, connect to CK810E SEL0 input, connect to GMCH LMD29 pin via 10 KΩ series resistor. **Case 2**, 100/133MHz support: 220 Ω pullup resistor to 3.3V, connect to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD.
BSEL1	I/O	220 Ω pullup resistor to 3.3V, connect to CK810E REF pin via 10 KΩ series resistor, connect to GMCH LMD13 pin via 10KΩ series resistor.
EMI[5:1]	I	Tie to ground. 0 Ω resistors are an option instead of direct connection to ground.

Table 8-8. Miscellaneous Checklist for SC242 Processors (Continued)

CPU Pin	I/O	Comments
PICCLK	I	Connect to clock generator / 22-33 Ω series resistor (though OEM needs to simulate based on driver characteristics).
SLOTOCC#	O	Tie to ground, leave it No Connect, or could be connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 KΩ–10 KΩ pullup resistor to any voltage.
TESTHI	I	1 KΩ–100 KΩ pullup resistor to VCC_2.5. If a legacy design pulls this up to VCC_{CORE}, use a 1 KΩ–10 KΩ pullup resistor.
THERMDN	O	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
THERMDP	I	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
VCC_CORE	I	Connect to core voltage regulator. Provide low frequency decoupling.
VID[4:0]	O	Connect to on-board VR or VRM. For on-board VR, 10 KΩ pullup resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pullups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
Vtt	I	Connect to 1.5V regulator. Provide high and low frequency decoupling.
NO CONNECTS	N/A	The following pins must be left as no-connects: A16, A47, A88, A113, A116, B12, B20, B76, B112.

Table 8-9. Special Consideration Checklist

Checklist Line Items	Comments
GND (VSS)	Connect AJ3, AL1, and AN3 to ground (Vss). These pins must be grounded.

Table 8-10. Clock Generator Checklist

Checklist Line Items	Comments
CPU	Series resistor 33 Ω ± 5%.
SDRAM/DCLK	Series resistor 22 Ω ± 5%. DCLK cap: 22 pF ± 2%.
3V66	Series resistor 22 Ω ± 5%. cap: 18pF ± 2%.
PCI	Series resistor 33 Ω ± 5%.
TCLK	Series resistor 22 Ω ± 5%.
OCLK/RCLK	Series resistor 33 Ω ± 5%.
48MHz	Series resistor 33 Ω ± 5%.
APIC	Series resistor 33 Ω ± 5%.
REF	Series resistor 10 Ω ± 5%.

Table 8-11. ICH Checklist

Checklist Line Items	Comments
PME#, PWRBTN#, LAD[3:0]#/FWH[3:0]#	No external pullup resistors on those signals with integrated pullups.
SPKR	Optional strapping: Internal pullup resistor is enabled at reset for strapping; after reset, the internal pullup resistor is disabled. Otherwise, connect to motherboard speaker logic.
AC_SDOUT	Optional strapping: Internal pulldown resistor is enabled at reset for strapping. after reset, the internal pulldown resistor is disabled. Otherwise, connect to AC'97 logic.
AC_BITCLK	Internal pulldown resistor is enabled only when the AC link shut-off bit in the ICH is set. Otherwise, connect to AC'97 logic.
AC_SDIN[1:0]	Internal pulldown resistors are enabled only when the AC link shut-off bit in the ICH is set. Use 10K ohm (approximate) pulldown resistors on both signals if using AMR. For onboard AC'97 devices, use a 10K ohm (approximate) pulldown resistor on the signal that is not used. Otherwise, connect to AC'97 logic.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors on those signals with integrated series resistors.
PCIRST#	The PCIRST# signal should be buffered to the IDE connectors.
No floating inputs (including bi-directional signals):	Unused core well inputs should be tied to a valid logic level (either pulled up to 3.3V or pulled down to ground). Unused resume well inputs must be either pulled up to 3.3VSB or pulled down to ground. Ensure ALL unconnected signals are OUTPUTS ONLY!
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10 KΩ (approximate) pulldown resistor. No other pullups/pulldowns are required. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Use approximately 1 KΩ pullup resistor to 5V.
PDDREQ, SDDREQ	Use approximately 5.6 KΩ pulldown resistor to ground.
IRQ14, IRQ15	Need 8.2K ohm (approximate) pullup resistor to 5V.
HL11	No pullup resistor required. A test point or no-stuff resistor is needed to be able to drive the ICH into NAND tree mode for testing purposes.
VccRTC	No Clear CMOS Jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe-mode strapping for Clear CMOS.
SMBus: SMBCLK SMBDATA	The SMBus signals can be pulled up to VCC3.3 standby. Isolate any devices that are not on the same power plane as the SMBus pullups in any states where VCC3.3 standby is on and VCC3.3 is off. The value of the SMBus pullups should reflect the number of loads on the bus. For most implementations with 4–5 loads, 4.7 KΩ resistors are recommended. OEMs should conduct simulation to determine exact resistor value.

Table 8-11. ICH Checklist (Continued)

Checklist Line Items	Comments
APICD[0:1], APICCLK	If the APIC is used: 150 Ω (approximate) pullups on APICD[0:1] and connect APICCLK to the clock generator. If the APIC is not used: The APICCLK can either be tied to GND or connected to the clock generator, but not left floating.
ICH RTC Oscillator Circuitry:	Refer to the circuit (resistor values and capacitor values, etc.) shown in the Design Guide.
GPI[8:13]	Ensure all wake events are routed through these inputs. These are the only GPIs that can be used as ACPI compliant wake events because they are the only GPI signals in the resume well that have associated status bits in the GPE1_STS register.
HL_COMP	There are 2 options for HL_COMP: **Option 1**–RCOMP Method: Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pullup resistor to 1.8V via a 10 mil wide, very short (~0.5 inch) trace (targeted for a nominal trace impedance of 40 Ω). **Option 2**–ZCOMP Method: The COMP pin must be tied to a 10 mil trace that is AT LEAST 18 inches long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.
5V_REF	Refer to the most recent version of the Design Guide for implementation of the voltage sequencing circuit.
SERIRQ	Need 8.2 KΩ (approximate) pullup resistor to 3.3V.
SLP_S3#, SLP_S5#	No pullups required. These signals are always driven by the ICH.
CLK66	Needs 18 pF tuning capacitor as close as possible to ICH.
PCI_GNT# signals	No external pullups are required on PCI_GNT# signals. However, if external pullups are implemented, they must be pulled up to 3.3V.

Table 8-12. ICH Checklist

Checklist Line Items	Comments
GPIO27/ALERTCLK GPIO28/ ALERTDATA	Add a 10 KΩ pullup resistor to 3VSB (3 volt standby) on both of these signals.

Table 8-13. GMCH Checklist

Checklist Line Items	Comments
VCCDA	VCCDA needs to be connected to an isolated power plane.
HCLK, SCLK	22 pF cap to ground as close as possible to GMCH.
GTLREFA, GTLREFB	Refer to the latest design guide for the correct GTLREF generation circuit.
HUBREF	Refer to the latest design guide for the correct HUBREF generation circuit. Also, place a 0.1 uF cap as close as possible to GMCH to ground.
IWASTE	Tie to ground.
IREF	Place a resistor as close as possible to GMCH and via straight to VSS plane. A 174 ohm 1% resistor is recommended.
LTVCA, LTVDA	10K ohm (approximate) pullup resistor to 3.3V if digital video out is not implemented.
TCLK	Series resistor 22 ohm ± 2%.
OCLK/RCLK	Series resistor 33 ohm ± 2%.
LMD[27:31] Reset strapping options:	Strapping options: For a “1”, use a 10K ohm (approximate) pullup resistor to 3.3V; a “0” is default (due to internal pulldown resistors). LMD31: 0 - Normal operation 1 - XOR TREE for testing purposes LMD30: 0 - Normal operation 1 - Tri-state mode for testing purposes (will tri-state all signals) LMD29: 0 - System bus frequency = 66 MHz 1 - System bus frequency = 100 MHz LMD28: The value on LMD28 sampled at the rising edge of CPURST# reflects if the IOQD (In-Order Queue Depth) is set to 1 or 4. 0 - IOQD = 4 1 - IOQD = 1 LMD27: Connect to $V_{CORE_{DET}}$ on the processor (pin E21) through a 10K ohm series resistor.
HCOMP	**Option 1**–RCOMP Method: Tie the HCOMP pin to a 40 ohm 1% or 2% (or 39 ohm 1%) pull-up resistor to 1.8V via a 10 mil wide, very short (~0.5”) trace. **Option 2**–ZCOMP Method: The HCOMP pin must be tied to a 10 mil trace that is AT LEAST 18” long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

Table 8-14. System Memory Checklist

Checklist Line Items	Comments
Pin 147	Connect to Ground (since Intel® 810E Chipset does not support registered DIMMs).
WP (Pin 81 on the DIMMs)	Add a 4.7K ohm pullup resistor to 3.3V. This is a recommendation to write-protect the DIMM’s EEPROM.
MAA[7:4], MAB[7:4]	Add 10 ohm series resistors to the MAA[7:4], MAB[7:4] as close as possible to GMCH for signal integrity.

Table 8-15. Display Cache Checklist

Checklist Line Items	Comments
CKE	4.7K ohm pull-up resistor to VCC3.

Table 8-16. LPC Super I/O Checklist

Checklist Line Items	Comments
LPC_PME#	Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH.
LPC_SMI#	This signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
LFRAME#	This signal is actively driven by ICH and does not require a pullup resistor.
LAD[0:3]	No additional pull-up resistors required. These signals have integrated pullups in the ICH.
LDREQ[0]#	This signal is actively driven by the Super I/O and does not require a pullup resistor.

Table 8-17. IDE Checklist

Checklist Line Items	Comments
CBLID#/PDIAG# (cable detect):	Refer to the latest design guide for the correct circuit. NOTE: All ATA66 drives will have the capability to detect cables.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors required on those signals with integrated series resistors.
IDE Reset	This signal requires a 22–47 ohm series termination resistor and should be connected to buffered PCIRST#.
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10K ohm (approximate) pull-down resistor to ground. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Need 1K ohm (approximate) pull-up resistor to 5V.
IRQ14, IRQ15	Need 8.2K ohm to 10K ohm pull-up resistor to 5V.
PDDREQ, SDDREQ	Need 5.6K ohm (approximate) pull-down resistor to ground.
CSEL	Need 470 ohm (approximate) pull-down resistor to ground.
IDEACTP#, IDEACTS#	Can use a 10K ohm (approximate) pull-up resistor to 5V for HD LED implementation.
IOCS16#	Leave as No Connect.

Table 8-18. Clock Generator Checklist

Checklist Line Items	Comments
VDD3 Pins	Each of the following groups of pins (all belonging to VDD3) need to be on their own isolated 3.3V power plane: Group 1: VCC3 pins 2, 9, 10 and 21 Group 2: VCC3 pin 27 Group 3: VCC3 pins 33, 38 and 44 (also SEL1)
CPU	Series resistor 33 ohm ± 5%.
SDRAM	Series resistor 22 ohm ± 5%.
DCLK	Series resistor 33 ohm ± 5%. DCLK cap: 22pF ± 2%
3V66	Series resistor 22 ohm ± 5%. 3V66 cap: 18pF ± 2%
PCI	Series resistor 33 ohm ± 5%.
TCLK	Series resistor 22 ohm ± 5%.
OCLK/RCLK	Series resistor 33 ohm ± 5%.
48MHz	Series resistor 33 ohm ± 5%.
APIC	Series resistor 33 ohm ± 5%.
REF	Series resistor 10 ohm ± 5%.

Table 8-19. FWH Checklist

Checklist Line Items	Comments
No floating inputs.	Unused FGPI pins need to be tied to a valid logic level.
INIT#	FWH INIT# must be connected to processor INIT#.
RST#	FWH RST# must be connected to PCIRST#.
ID[3:0]	For a system with only one FWH device, tie ID[3:0] to ground.

Table 8-20. PCI Bus Checklist

Checklist Line Items	Comments
ACK64# REQ64#	(5V PCI environment) 2.7K ohm (approximate) pull-up resistors to VCC5. (3V PCI environment) 8.2K ohm (approximate) pull-up resistors to VCC3_3. Each REQ64# and ACK64# requires its own pull-up.
IDSEL lines to PCI connectors	100 ohm series resistor.
SBO# SDONE	5.6K ohm pull-up resistor to VCC3_3 or VCC5.
3Vaux	Optional to 3VSB, but required if PCI devices supporting wakeup events.

Table 8-21. USB / Keyboard / Mouse Checklist

Checklist Line Items	Comments
D-/D+ data lines	To provide nominal target trace impedance of 45 ohm, should be 9 mils wide based on the recommended stackup presented in Section 4.2, “Nominal Board Stackup” on page 4-1.
D-/D+ data lines	Use 15 ohm series resistors.
VCC USB (Cable power)	Power off 5 volt standby, if wake on USB is to be implemented, If there is adequate standby power. It should be powered off of 5 volt core instead of 5 volt standby if adequate standby power is not available.
Voltage Drop Considerations	The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and Power/GND trace width. This must be done such that the resistance between the Vcc5 power supply and the host USB Port is minimized. Minimizing this resistance will minimize voltage drop seen along that path during operating conditions.
Fuse	A minimum of 1A fuse should be used. A larger fuse may be necessary to minimize the voltage drop.
Voltage Droop Considerations	Sufficient bypass capacitance should be located near the host USB receptacles to minimize the voltage droop that occurs upon the hot attach of a new device. See the most recent version of the USB specification for more information.

Table 8-22. AC’97 Checklist

Checklist Line Items	Comments
AC_SDIN[1:0]	AC_SDIN[0] is recommended to be used for an onboard audio codec. Only one primary codec can be present on the link. A maximum of two active codecs are supported in an ICH platform. The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10K ohm) pull-down resistor (See Section 4.9, “AC’97” on page 4-19 for more information).
PRI_DN#	If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground. The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
AC-link	Components such as FET switches, buffers, or logic gates, should not be implemented on the AC-link signals, except AC_RST#, without doing thorough simulation and analysis. Doing so will potentially interfere with timing margins and signal integrity A means of preventing contention on the AC-link must be provided for an onboard codec if the motherboard requires that an AMR module with a primary codec take precedence over an onboard primary codec.
AUDIO_MUTE#:	No connect on the motherboard.
AUDIO_PWRDN	Codecs on the AMR card should implement the EAPD powerdown pin, per the AC’97 2.1 specification, to control the amplifier.
MONO_PHONE	Connect to onboard audio codec if supported.
MONO_OUT/ PC_BEEP	Connect to SPKR output from ICH or MONO_OUT from onboard codec.
PRIMARY_DN#	See discussion above.

Table 8-22. AC'97 Checklist (Continued)

Checklist Line Items	Comments
+5VDUAL/+5VSB	If an adequate power supply is available, this pin should be connected to +5Vdual or +5Vsby. In the event that these planes cannot support the required power, it can be connected to VCC5 core on the motherboard. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
S/P-DIF_IN	Connect to ground on the motherboard.
AC_SDIN[3:2]	No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDIN[1:0].
AC97_MSTRCLK	Connect to ground on the motherboard.
PC_BEEP	Should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

Table 8-23. Power Delivery Checklist

Checklist Line Items	Comments
All voltage regulator components meet maximum current requirements	Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements	Ensure the voltage regulator components and dissipate the required amount of heat.
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	"Dual" voltage rails may not be at the expected voltage.
Dropout Voltage	The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met	See individual component specification for each voltage tolerance.
Total power consumption in S3 must be less than the rated standby supply current.	Adequate power must be supplied by power supply.

8.2 Pullup and Pulldown Resistor Values

Pullup and pulldown values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pullup voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pullup voltage tolerance, the pullup/pulldown resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications and other considerations.

A simplistic DC calculation for a pullup value is:

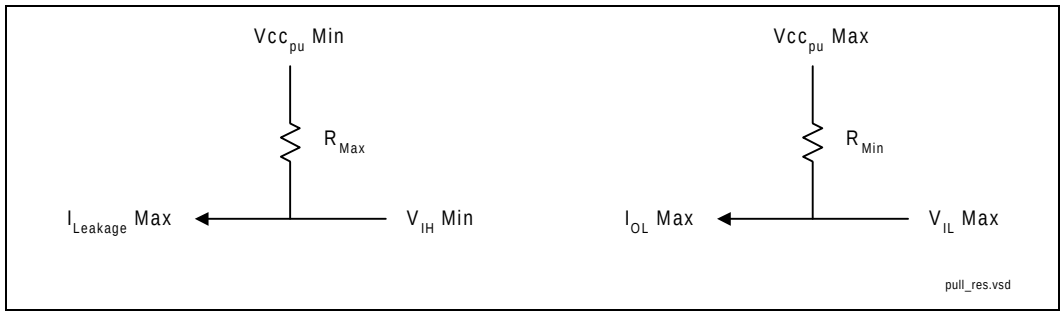
$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

$$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} is also determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including input capacitance of the devices to be driven, output capacitance of the driver, and line capacitance. This calculation yields the largest pullup resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * ln(1-(V_{IH}\ MIN / Vcc_{PU}\ MIN)\ )\ )$$

Figure 8-1. Pullup Resistor Example



8.3 RTC

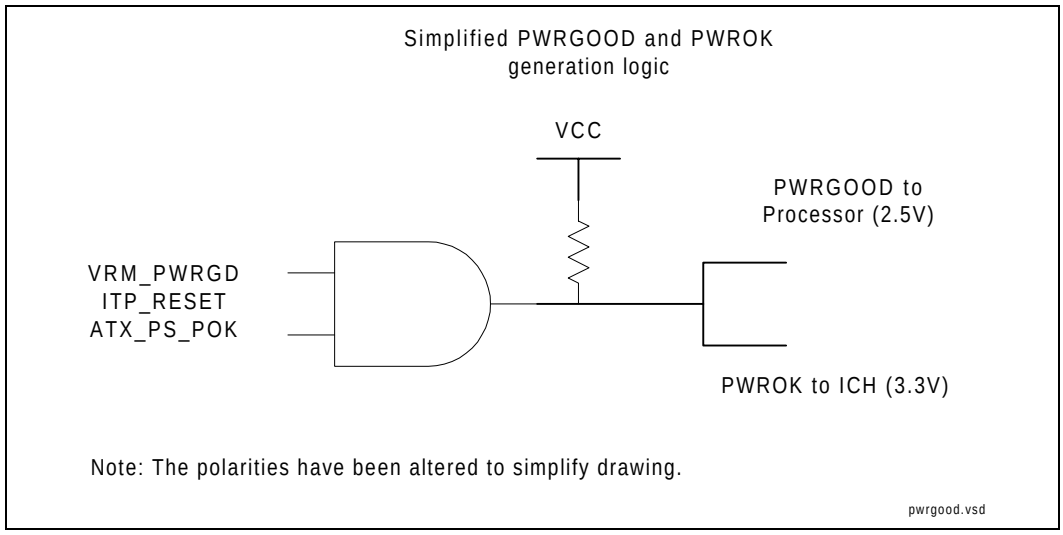
Guidelines to minimize ESD events that may cause loss of CMOS contents:

- Provide a 1 uF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. This capacitor connection should not be stubbed off the trace run and should be as close as possible to the ICH. If a stub is required, it should be kept to a few mm maximum length. The ground connection should be made through a via to the plane with no trace between the capacitor pad and the via.
- Place the battery, 1K ohm series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1K ohm resistor as close to the 1 µF cap as possible. Do not place these components between the cap and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis-intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.
- Keep the ICH VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by those handling the board.

8.4 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16 msec debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity, and not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, making sure that the input to the ICH is at a 3V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 msec.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to CPU is driven with an open collector buffer pulled up to 2.5V using a 330 ohm resistor.
- The circuitry checks for both processor VRM powered up, and the PS_POK signal from the ATX power supply connector before asserting PWRGOOD and PWROK to the processor and ICH.

Figure 8-2. PWRGOOD and PWROK Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

8.4.1 Power Button Implementation

The items below should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1–Stop Grant – (CPU context not lost)

S3–STR (Suspend To RAM)

S4–STD (Suspend To Disk)

S5–Soft-off

- Wake: Pressing the power button wakes the computer from S1–S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
  - — If SCI is enabled, the power button will generate an SCI to the OS.
    - The OS will implement the power button policy to allow orderly shutdowns.
    - Do not override this with additional hardware.
  - — If SCI is not enabled:
    - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
    - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
    - Always install an SMI handler for the power button that operates until ACPI is enabled.
  - — Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
    - This is only to be used in EMERGENCIES when system is not responding.
    - This will cause the user data to be lost in most cases.
    - Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off; this violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear off to the user when in the S1–S4 sleeping states. This includes:
  - — All lights except a power state light must be off.
  - — The system must be inaudible: silent or stopped fan; drives are off.

Note: Contact Microsoft* for the latest information concerning PC9x and Microsoft* Logo programs.



9

Flexible Motherboard Guidelines

Flexible Motherboard Guidelines 9

9.1 Flexible Processor Guidelines

9.1.1 Flexible System Design DC Guidelines

The processor DC guidelines for flexible system designed in this section are defined at the processor pin.

Table 9-1 lists the guidelines for future 1.5V processors and Table 9-2 lists the guidelines for future 2.0V processors. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 9-1. Flexible Processor Voltage and Current Guidelines for 1.5V Processors

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vcc_{CORE}	V_{CC} for processor core		1.5		V	1, 3
Baseboard Tolerance, Static	processor core voltage static tolerance at processor pins	–0.070		0.070	V	2, 3
Baseboard Tolerance, Transient	processor core voltage transient tolerance level at processor pins	–0.110		0.110	V	2, 3
I_{CCCORE}	I_{CC} for processor core			12.6	A	1, 4, 5, 7
I_{SGnt}	I_{CC} Stop-Grant for processor core			0.8	A	6
dI_{CCCORE}/dt	Power supply current slew rate			240	A/µS	8, 9

NOTES:
1. Vcc_{CORE} and Icc_{CORE} supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the processor pin at the bottom side of the system platform. Vcc_{CORE} must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc max. voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

   $$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE}\ \text{Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum Vcc_{CORE}.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

Table 9-2. Flexible Processor Voltage and Current Guidelines for 2.0 V Processors [1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vcc_{CORE}	V_{CC} for processor core		2.00		V	1, 3
Baseboard Tolerance, Static	processor core voltage static tolerance at processor pins	–0.089		0.100	V	2, 3
Baseboard Tolerance, Transient	processor core voltage transient tolerance level at processor pins	–0.144		0.144	V	2, 3
I_{CCCORE}	I_{CC} for processor core			15.6	A	1, 4, 5, 7
I_{SGnt}	I_{CC} Stop-Grant for processor core			0.8	A	6
dI_{CCCORE}/dt	Power supply current slew rate			240	A/µS	8, 9

NOTES:

1. Vcc_{CORE} and Icc_{CORE} supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the top of the PPGA package. Vcc_{CORE} must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc max. voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e. typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

   $$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE}\ \text{Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum Vcc_{CORE}.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

9.1.2 System Bus AC Guidelines

Table 9-3 and Table 9-4 contain 66 MHz and 100 MHz system bus AC Guidelines defined at the processor pins.

Table 9-3 contains the BCLK guidelines and Table 9-4 contains the AGTL+ system bus guidelines. Processor System Bus AC Specifications for the AGTL+ Signal Group at the processor pins for 100 MHz are equivalent to 66 MHz. The 66 MHz specification is documented in the processor datasheet.

Table 9-3. Flexible Motherboard Processor System Bus AC Guidelines (Clock) at the Processor Pins [1,2,3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency			66.67 100.00	MHz MHz		All processor core frequencies
T1: BCLK Period	15.0 10.0			ns ns	9-1 9-1	4, 5, 9 4, 6, 9
T2: BCLK Period Stability			±300 ±250	ps ps	9-1 9-1	5, 7, 8, 9 6, 7, 8, 9
T3: BCLK High Time	4.94 2.5			ns	9-1	@>2.0V [5] @>2.0V [6]
T4: BCLK Low Time	4.94 2.4			ns	9-1	@<0.5V [5] @<0.5V [6]
T5: BCLK Rise Time	0.34 0.38		1.5 1.36	ns ns	9-1 9-1	(0.5V–2.0V) [5, 11] (0.5V–2.0V) [6, 11]
T6: BCLK Fall Time	0.34 0.38		1.5 1.36	ns ns	9-1 9-1	(2.0V–0.5V) [5, 11] (2.0V–0.5V) [6, 11]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25V at the processor core pins.
4. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
5. This specification applies to the processor when operating with a system bus frequency of 66 MHz.
6. This specification applies to the processor when operating with a system bus frequency of 100 MHz.
7. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
8. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 KHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
9. The average period over a 1uS period of time must be greater than the minimum specified period.

Figure 9-1. BCLK Waveform

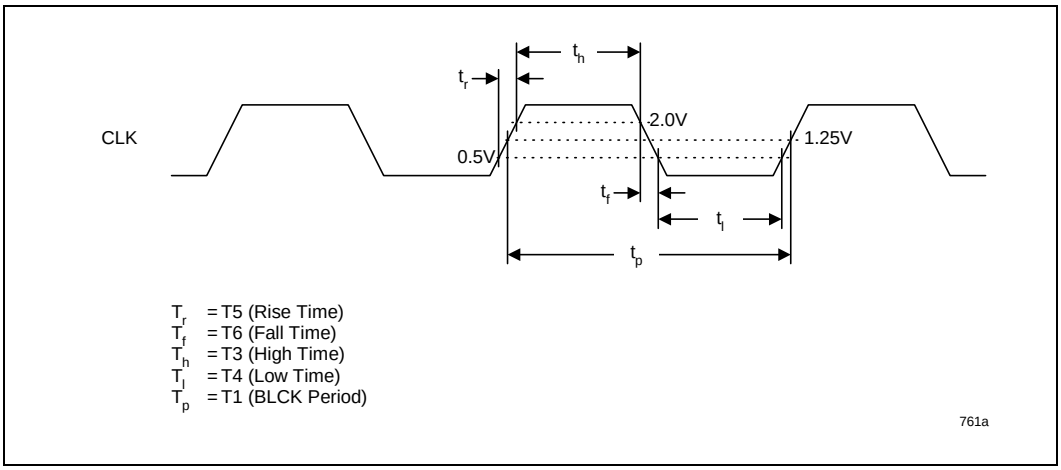


Table 9-4. Processor System Bus AC Guidelines (AGTL+ Signal Group) at the Processor Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.30	4.43	ns	9-2	5
T8: AGTL+ Input Setup Time	1.75		ns	9-3	5, 6, 7, 8
T9: AGTL+ Input Hold Time	0.85		ns	9-3	9
T10: RESET# Pulse Width	1.00		ms	9-4	7, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz or 100 MHz system bus.
5. Valid delay timings for these signals are specified into 25 ohm to 1.5V and with V_{REF} at 1.0V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40V swing.
9. Specification is for a maximum 1.0V swing.
10. After Vcc_{CORE} and BCLK become stable.

Figure 9-2. Processor System Bus Valid Delay Timings

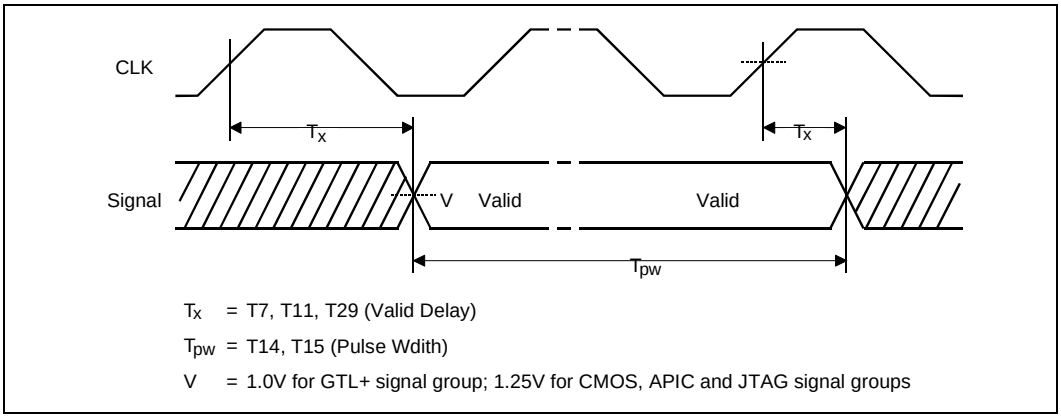


Figure 9-3. Processor System Bus Setup and Hold Timings

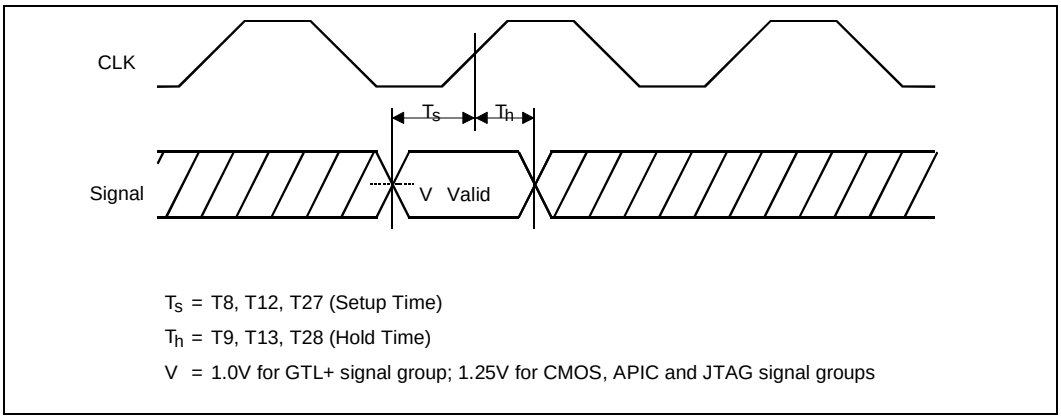
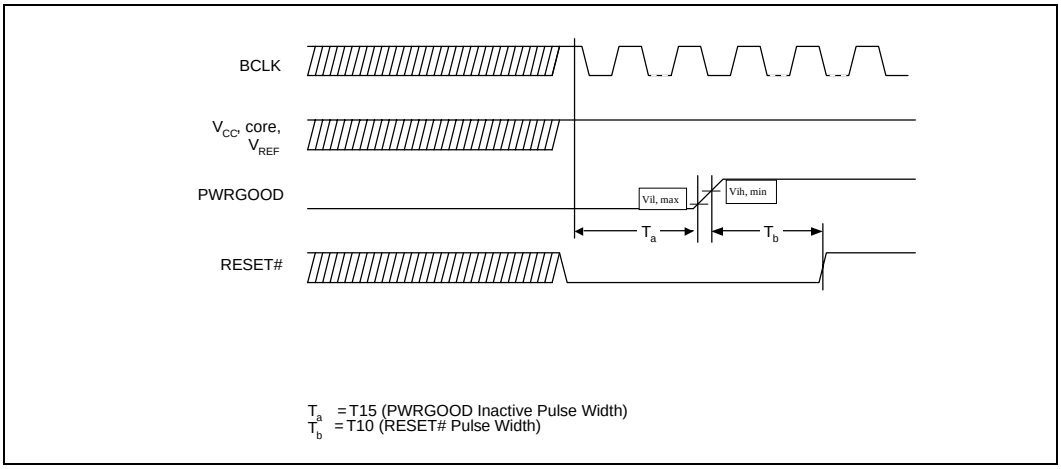


Figure 9-4. Power-On Reset and Configuration Timings



9.1.3 Thermal Guidelines

Table 9-5 provides the recommended thermal design power dissipation for use in designing a flexible system board. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are specified in Table 9-5. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

Table 9-5. Intel® Celeron™ Processor PPGA Flexible Thermal Design Power [1, 2]

Processor Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)
30.0[2]	0	70

NOTES:
1. These values are specified at nominal Vcc_{CORE} for the processor core.
2. These values are preliminary.





10

Third Party

Third-Party Vendor Information 10

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the Intel® 810E Chipset. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Table 10-1. Super I/O

Vendors	Contact	Phone
SMC	Dave Jenoff	(909) 244-4937
National	Robert Reneau	(408) 721-2981
ITE	Don Gardenhire	(512)388-7880
Winbond	James Chen	(02) 27190505 - Taipei office

Table 10-2. Clock Generation

Vendors	Contact	Phone
Cypress	John Wunner	206-821-9202 x325
ICS	Raju Shah	408-925-9493
IC Works	Jeff Keip	408-922-0202, x1185
IMI	Elie Ayache	408-263-6300, x235
PERICOM	Ken Buntaran	408-435-1000

Table 10-3. Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Table 10-4. Voltage Regulator Vendors

Vendors	Contact	Phone
Linear Tech Corp.	Stuewart Washino	408-432-6326
Celestica	Dariusz Basarab	416-448-5841
Corsair Microsystems	John Beekley	888-222-4346
Delta Electronics	Colin Weng	886-2-6988, x233(Taiwan)
N. America: Delta Products Corp.	Maurice Lee	510-770-0660, x111

Table 10-5. Flat Panel

Vendors	Contact	Phone
Silicon Images Inc	Vic Decosta	408-873-3111

Table 10-6. TV-Out

Vendors	Contact	Phone
Chrontel	Ted Friedland	408-544-217

Table 10-7. Software DVD

Vendors	Contact	Phone
Ravisert	Pete Nush	610-251-9999 x 745
Intervideo	Joe Monisero	510-651-08888 x 102
M6ISoft (Zoran)	Paul Farrelle Mike Redding	408-919-4000 408-919-4224
Media	Partha Srinvasan	510-668-4850 x 202
Cyberlink	Alex Weng	886-2-8667-1298

Table 10-8. AC'97

Vendors	Contact	Phone
Analog Devices	Dave Babicz	781-461-3237
AKM	George Hill	408-436-8580
Cirrus Logic (Crystal)	David Crowell	512-912-3587
Creative Technologies Ltd./ Ensoniq Corp.	Steve Erickson	408-428-6600 x6945
Diamond Multimedia Systems	Theresa Leonard	360-604-1478
ESS Technology	Bill Windsor	510-492-1708
Euphonics, Inc.	David Taylor	408-554-7201
IC Ensemble Inc.	Steve Allen	408-969-0888 x106
Motorola	Pat Casey	508-261-4649
PCTel, Inc.	Steve Manuel	410-965-2172
Conexant (formerly Rockwell)	Tom Eichenberg	949-221-4164
SigmaTel	Spence Jackson Arron Lyman	512-343-6636 512-343-6636 x11
Staccato Systems	Bob Starr	650-853-7035
Tritech Microelectronics, Inc.	Rod Maier	408-941-1360
Yamaha	Jose Villafuerte (US) Kazunari Fukaya (Japan)	408-467-2300 (0539) 62-6081



A

PCI Devices/Functions/ Registers/Interrupts

PCI Devices/Functions/Registers/ Interrupts A

Table A-1. PCI Devices and Functions

Device	Function	Function Description
82801AA (ICH)		
Device 30	Function 0	Intel® 82801AA PCI Bridge
Device 31	Function 0	Intel® 82801AA LPC Bridge
Device 31	Function 1	Intel® 82801AA Bus Master IDE Controller
Device 31	Function 2	Intel® 82801AA USB Universal Host Controller
Device 31	Function 3	Intel® 82801AA SMBus Controller
Device 31	Function 4	Reserved
Device 31	Function 5	Intel® 82801AA AC'97 Audio Controller
Device 31	Function 6	Intel® 82801AA AC'97 Modem Controller
Device 31	Function 7	Reserved
82810E GMCH		
Device 0	Function 0	Intel® 82810E System and Memory Controller
Device 1	Function 0	Intel® 82810E Internal Graphics Device

Table A-2. PCI Devices and Registers

Function Description	Vendor ID Register	Device ID Register	Revision ID Register	Class Code Register	Sub-Class Register	Program Interface Register
82801AA (ICH)						
PCI Bridge	8086h	0x2418	Note 1	06h	04h	00h
LPC Bridge	8086h	0x2410	Note 1	06h	01h	00h
Bus Master IDE Controller	8086h	0x2411	Note 1	01h	01h	80h
USB Universal Host Controller	8086h	0x2412	Note 1	0Ch	03h	00h
SMBus Controller	8086h	0x2413	Note 1	0Ch	05h	00h
AC'97 Audio Controller	8086h	0x2415	Note 1	04h	01h	00h
AC'97 Modem Controller	8086h	0x2416	Note 1	04h	01h	00h
82810E GMCH						
System and Memory Controller	8086h	0x7124	Note 1	06h	00h	00h
Internal Graphics Device	8086h	0x7125	Note 1	03h	00h	00h

NOTES:
1. See Specification Update document for the particular product.

Table A-3. PCI Devices and Interrupts

Function Description	APIC Interrupt	ISA/PCI IRQ
82801AA (ICH)		
Intel® 82801AA PCI Bridge	N/A	N/A
Intel® 82801AA LPC Bridge	N/A	N/A
Intel® 82801AA Bus Master IDE Controller	Interrupt 14	IRQ14
Intel® 82801AA USB Universal Host Controller	Interrupt 18	PIRQC#
Intel® 82801AA SMBus Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
Intel® 82801AA AC'97 Audio Controller	Interrupt 17	PIRQB#
Intel® 82801AA AC'97 Modem Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
82810E GMCH		
Intel® 82810E System and Memory Controller	N/A	N/A
Intel® 82810E Internal Graphics Device	Interrupt 16	PIRQA#